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Growth of germanium nanowires using industry-benign catalysts

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GROWTH OF GERMANIUM NANOWIRES USING INDUSTRY-BENIGN CATALYSTS

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ABSTRACT

GROWTH OF GERMANIUM NANOWIRES USING INDUSTRY-BENIGN CATALYSTS

by Gabriel Calebotta

Elemental germanium nanowires were successfully grown on both Si(111) and SiO_2 substrates using indium or antimony as catalysts. The nanowires were grown in a 1" diameter quartz tube by depositing vaporized germanium onto the substrates at specific temperatures. The nanowires were characterized using scanning electron microscopy, transmission electron microscopy, energy dispersive spectroscopy, and electron diffraction. The highest average surface density of nanowires, 28.5 μm^{-2}, was recorded on SiO_2 substrates, coated with 30 nm of indium, and processed at 450 °C. The average diameter of indium-catalyzed germanium nanowires was found to be 15 nm. Antimony-catalyzed germanium nanowires grew with a beaded morphology making accurate measurements of their diameters impossible. High resolution transmission electron microscope images and electron diffraction patterns indicated the wires had a diamond cubic crystal structure and grew along the <111> crystallographic direction. Lattice parameter measurements and energy dispersive spectroscopy measurements confirmed the wires were elemental germanium.

ACKNOWLEDGMENTS

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Table of Contents

List of Figures

List of Tables

CHAPTER ONE

INTRODUCTION

Research in the synthesis of nanostructures, or structures with at least one dimension below 100 nm, has attracted much interest due to their unique physical properties. Electrons within nanostructures exhibit quantum confinement, causing the electrons to exist in discreet energy levels rather than in a broad spectrum of energies as seen in traditional materials. Theoretically, by adjusting the size of a nanostructure, it is possible to engineer its specific electrical, optical, and magnetic properties. However, the method of manufacturing nanostructures is significantly different from traditional manufacturing techniques. Nanostructures are grown by controlling the thermodynamics and kinetics of a process, causing the atoms to arrange themselves in a desired configuration. It is this aspect of nanostructures that is of particular interest to the semiconductor industry.

In 1954, Gordon Moore, co-founder of Intel, stated that the number of transistors per unit area on an integrated circuit would double every year [1]. This estimate was later revised to every eighteen months and became known as Moore's Law. Because semiconductor manufacturing relies on photolithography, the smallest device feature size achievable is limited by the wavelength of the light used in the photolithographic process. The current projection for the absolute minimum feature size is 32 nm, which is expected to be in production in the first half of the next decade. Once this size has been reached, new processing techniques for device synthesis must be developed to continue increasing device densities. Because nanostructures are grown atom by atom rather than etched as

in traditional semiconductor manufacturing techniques, they offer the possibility of extending Moore's Law beyond the limits of photolithography.

Growth of nanostructures has been documented since the late 1970's when nanowires with uniform diameters of 20 nm were grown through vapor phase deposition of poly-(sulphur nitride). At that time, these wires were viewed as an annoying artifact, and minimizing their growth was the priority [2].

More recently, the usefulness of quantum structures has been recognized. Increasingly intricate two dimensional structures have been constructed due to advances in molecular beam epitaxy [3]. These structures, known as quantum wells, consist of stacks of alternating layers of semiconductor materials that are less than 100 nm thick. Quantum wells have been particularly successful in optoelectronics, where they have been available commercially as edge emitting lasers and light emitting diodes (LEDs) beginning in the late 1990's. Research in zero dimensional quantum structures, or quantum dots, followed the development of quantum wells. The synthesis of quantum dots allowed for a more detailed study of the physics of small sizes and they have been used in the construction of a number of devices. In particular, quantum dots have been used in lasers, LEDs, and single electron transistors [3].

Research in one dimensional structures followed research in quantum wells and quantum dots. One dimensional structures provide a promising platform for studying the relationship between size and quantum confinement of electrons. Most of the research in one dimensional structures of the last decade has focused on carbon nanotubes. Semiconductor nanowires, or single crystal semiconductor whiskers, have recently

attracted attention because they would be easier to integrate into existing semiconductor devices, compared to integrating carbon nanotubes. Despite their potential as a solution to the limitations of conventional integrated circuit processing, nanowires have only been successfully fabricated in the laboratory. More work needs to be done to develop manufacturing processes that not only ensure high yields but can also be readily integrated into existing semiconductor manufacturing processes.

Semiconductor nanowires have been grown with most of the elemental and common compound semiconductors. Germanium (Ge) has recently gained a new level of interest due its higher electron-hole mobility as compared to Si. This has led to an interest in Ge nanowires for high performance memory applications. In addition, Ge has a larger excitonic Bohr radius than Si, which would make quantum confinement effects easier to observe in Ge nanowires [4]. The majority of research in Ge nanowire growth is based on the vapor-liquid-solid (VLS) mechanism first demonstrated by Wagner and Ellis. In this process, a metal catalyst droplet is alloyed and supersaturated with vaporized Ge, resulting in precipitation and axial growth of a Ge nanowire beneath the droplet [2].

The majority of research in Ge nanowire growth has focused on Au catalyzed synthesis. This is because the Au-Ge system exhibits a low bulk eutectic temperature (363 °C) and no stoichiometric compounds, allowing relatively low temperature precipitation of 99.99991% pure Ge [5]. The use of Au as a catalyst poses a significant problem for integrating such nanowires into mainstream semiconductor processing because Au is seen as a contaminant and offers little to no useful properties to the nanowire after growth.

To facilitate the integration of Ge nanowires into practical applications, new industry-benign catalysts need to be thoroughly explored. Indium (In) and antimony (Sb), both commonly used for transistor channel or junction doping, were investigated as possible catalysts for Ge nanowire synthesis. Similar to Au, both exhibit eutectic behavior with Ge and there are no stoichiometric compounds in either the Ge-In or Ge-Sb binary system. In addition, In, with acceptor properties, and Sb, with donor properties, could potentially serve as the dopant sources for Ge nanowires. This would eliminate the need for additional processing steps after growth to successfully dope the wires, thus making them easier to incorporate into existing semiconductor devices.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

A detailed discussion of the relevant literature regarding Ge nanowire synthesis follows. This is organized in a manner to assist the development of a basic understanding of the fundamental aspects of nanowire synthesis. Section 2.2 of this review is an introduction to the vapor-liquid-solid growth mechanism that is used for Ge nanowire growth. It covers the basic phenomenon as well as its historical roots. In Section 2.3 the methods used to deposit Ge onto the substrate and the experimental conditions used by researchers are covered. The processing parameters for Ge nanowire growth and discusses the effects each parameter has on Ge nanowire growth and morphology are described in Section 2.4. The results from previous experiments and from the literature are compared and contrasted in Section 2.5.

2.2 History and Basic Description of the Vapor-Liquid-Solid Mechanism

The first experiments conducted with the vapor-liquid-solid mechanism, and the thermodynamic and kinetic requirements for it occur, are presented in this section.

2.2.1 Discovery of the Vapor Liquid Solid Mechanism

Wagner and Ellis first reported the growth of silicon whiskers with diameters from 1 μm to 0.2 mm in 1964 [2]. It was at this time that the vapor liquid solid (VLS) growth mechanism was recognized. This process begins by melting a metal thin film on

a substrate, causing it to agglomerate into droplets to reduce its surface energy. The droplets are then alloyed with another material which is introduced as a vapor. The vaporized material adsorbs onto and diffuses into the molten droplet. Once the droplet becomes saturated, any additional material that is absorbed causes nucleation of a precipitate. With Si and Ge, the precipitation occurs on the substrate beneath the molten droplet. As more material is added to the droplet, more material is precipitated out onto the substrate. As the area under the droplet fills up, a second layer is epitaxially added on top of the first. This process continues indefinitely, forming a whisker beneath the molten droplet [2].

Initial theories of VLS growth followed the Frank mechanism, where axial growth was predicated on a structural defect such as a screw dislocation. Webb *et al.* showed that this mechanism did not apply to all materials when they examined axial growth of nine metals and found definitive evidence of an axial dislocation only with palladium [6]. Wagner *et al.* confirmed that silicon whisker growth occurred without the presence of a line defect [2]. It was also concluded that axial growth proceeded in the <111> direction for Si.

2.2.2 Vapor Liquid Solid Growth

As stated in Section 2.2.1, whisker and nanowire growth occurs from a supersaturated alloy. The process itself can be broken down into four distinct stages [2].

1. The metal catalyst is melted and the growth material is vaporized and the two are brought into contact.

2. The vaporized material begins diffusing through the vapor-liquid interface and alloying with the catalyst.
3. The metal catalyst reaches saturation causing nucleation at the solid-liquid interface.
4. As more material is added to the molten droplet, layers are formed epitaxially beneath the catalyst, leading to axial growth.

This process is illustrated in Figure 1. This process is referred to as tip-led growth.

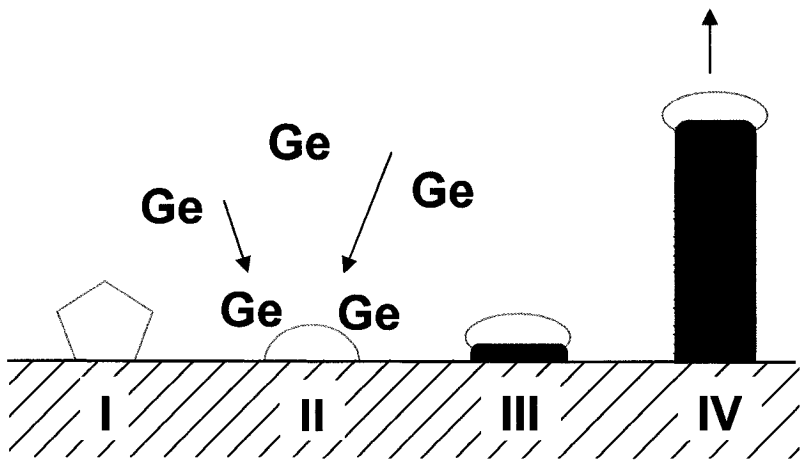

Figure 1. Diagram of VLS process for nanowire growth. Adapted from [7].

2.3 Ge Deposition Methods

Ge deposition has been carried out for Ge nanowire growth using four different methods. These are physical vapor deposition, pulsed laser deposition, chemical vapor deposition, and reduction of germanium containing supercritical solutions. A description of each method will be given in addition to experimental conditions and results reported in the relevant literature.

2.3.1 Physical Vapor Deposition

Physical vapor deposition (PVD) is by far the simplest of the deposition techniques used for synthesis of Ge nanowire. Powdered germanium (the source) is vaporized and carried to the substrate in a gas stream. The substrate is also heated, though at a significantly lower temperature than the source. The temperature of the substrate still has to be above the melting temperature of the catalyst to ensure the vaporized source will alloy with the catalyst. Typical carrier gases for PVD of Ge to grow Ge nanowires are argon and hydrogen.

Gu *et al.* utilized this method to grow Ge nanowires on silicon and silicon dioxide using Au thin films and nanoparticles as catalysts, respectively [8]. The wires were grown in the <111> axial direction regardless of the form of the catalyst or the crystallographic orientation of the substrate. Compositional analyses of the wires showed that they were comprised almost entirely of Ge with trace amounts of oxygen. The wires were also wrapped in a 2 nm thick germanium oxide sheath [8].

Despite its simplicity, PVD does have some significant drawbacks when compared to other deposition methods. Control of the deposition is more difficult than techniques such as chemical vapor deposition (CVD). This is because the vaporized material will solidify once it reaches a cooler temperature, which leads to a large portion of the vaporized material being deposited on the walls of the reactor or across the substrate.

2.3.2 Laser Ablation or Pulsed Laser Deposition

Pulsed Laser Deposition, or PLD, is a deposition method that uses a laser to sublimate a source material, which is then carried to a collection plate in a gas stream. The process is conducted under vacuum and in a heated furnace. The source is a block of material made from the same materials desired for the nanowires. The ablated material in the gas flow is then collected on a chilled plate, often called a cold finger [9].

Pulsed laser deposition (PLD) was first pioneered for nanowire synthesis by Morales and Lieber [9]. Their process used a pulsed Nd-yttrium-aluminum-garnet (Nd:YAG) laser with a characteristic wavelength of 532 nm. For Ge nanowire growth, Morales and Lieber used a $Ge_{0.9}Fe_{0.1}$ target. The furnace temperature was 820 °C. This temperature and atomic composition corresponds to the β-$FeGe_2$(s) + Ge(s) two phase region in the Ge-Fe binary system and is 18°C below the FeGe(l) + Ge(s) two phase region. The wires produced were oriented along the <111> direction and were comprised entirely of Ge. The catalyst tip was $FeGe_2$, as predicted by the phase diagram. The wires produced in this study did not have an oxide sheath which is commonly found when using other methods [9].

2.3.3 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is the decomposition of a gaseous precursor under tightly controlled temperatures and pressures. The decomposition of the precursor leaves a solid deposit on the substrate and a gaseous by-product which is removed. The solid deposit is typically a thin film or powder. This technique has been used for some

time in the semiconductor industry to deposit metals, ceramics, and semiconductors. The technique has also been used in different incarnations to deposit polymers. The reduction of silane (SiH_4) has been used extensively for the growth of Si nanowires [10]. Wagner and Ellis used $SiCl_4$ as the precursor for their original experiment on whisker growth [2].

Recently, CVD has been adopted as a viable means of producing high quality crystalline Ge nanowires as well. While Ge nanowires have been grown primarily by decomposing germane (GeH_4), other compounds, such as digermane (G_2H_8) and $Ge(C_5H_5)_2$, have also been used [11-17].

Wires grown using CVD have been oriented along the <111>, <110>, and <112> directions [6,7,15]. The latter of these three was the most unique and was only found using $Ge(C_5H_5)_2$ as a precursor on an Fe substrate. No catalyst was used in this process. The wires were synthesized using a self-seeding process in which the Ge alloyed with the substrate itself, forming nucleation sites from which the nanowires grew [18].

2.3.4 Supercritical Fluid Liquid Solid Synthesis

Supercritical fluid liquid solid synthesis (SFLS) is similar to CVD in that a Ge containing precursor is chemically decomposed to deposit Ge on the substrate. The precursors in this case were organogermanes such as diphenylgermane (DPG) or tetraethylgermane (TEG). Catalysts in the form of colloidal dispersions were mixed with the precursor, typically under an inert atmosphere. The precursor/catalyst solution was then injected into a reactor which is filled with hexane. The reactor was heated to 375 °C and pressurized to 20 MPa. The extremely high pressure within the reactor placed the

hexane above its critical point. A Si(100) substrate was placed within the reactor and collected the nanowires as they settled out of the solution. When the desired growth time elapsed, the reactor was depressurized and cooled and the reaction byproducts were flushed out with a clean inert gas. This method produced sizable quantities of single crystal Ge nanowires, on the order of milligrams. The wires produced using SFLS were oriented predominantly in the <110> and <111> directions [5,18].

2.4 Process Parameters

This section details the processing parameters that were examined in the relevant literature and their effects on the growth of Ge nanowires. The parameters discussed are temperature, pressure, substrate orientation, and choice of catalyst.

2.4.1 Temperature

Ge nanowires have been synthesized over a wide range of temperatures. For the most part, these temperatures fall well below the temperatures commonly used to grow Si nanowires. Most of the reported growth of Ge nanowires has been conducted close to the eutectic temperature of the Au-Ge binary system, which is 363 °C. However, growth has taken place at temperatures both significantly above and below this temperature.

Kamins *et al.* studied Ge nanowire growth at temperatures between 310 °C and 425 °C. Their results showed Ge nanowire growth only between 320-380 °C. Wires grown between 320 °C and 350 °C exhibited a slightly tapered diameter, the extent of which increased with increasing temperature. A tapered diameter is indicative of three

dimensional growth. Atoms from the vapor phase adsorb onto the existing wire as well as onto the molten catalyst tip. Wires grown at higher temperatures in their experiment, between 350-380 °C, exhibited six fold faceted faces, consistent with the <111> axial growth direction. In addition, the wires grown at these temperatures also had tapered diameters. At higher temperatures, the quality of the nanowires decreased and they began to resemble blocky irregular shapes as opposed to nanowires. At the highest temperature of 380 °C, these were the only structures present. The highest quality wires were grown at 320 °C [11].

In contrast to Kamins *et al.*, the research conducted by Wang *et al.* has shown that Ge nanowire growth can be carried out at 275 °C, 85 °C below the Au-Ge eutectic temperature [11-13]. This ultra-low temperature growth has been attributed to a suppressed Au-Ge eutectic temperature. It is thought that the Au-Ge eutectic temperature is decreased because of the decreased melting temperature of Au nanoparticles [12]. This concurs with published research on the suppressed melting temperature found in Au nanoclusters [19]. The wires grown at this temperature grew along the <110> direction.

At the other temperature extreme, Wu and Yang have grown Ge nanowires at comparatively high temperatures. They successfully grew wires with varying diameters at approximately 900 °C, very near the melting point of Ge, and reported that their wires grew along the <111> direction [7, 20].

From the three examples cited here, it appears that temperature plays a major role in determining the growth direction of the nanowires. This would be too broad of a statement. For example, though the <110> growth direction was found in nanowires

grown at 275 °C , it was also found in nanowires grown at 820 °C [9,12]. These two experiments were conducted at different pressures and with different methods of deposition. It would be more accurate to say that there are several factors that contribute to the direction of axial growth, one of which is temperature.

2.4.2 Pressure

Like temperature, there is a wide range of pressures present in the systems used to grow Ge nanowires because of the multiple methods used in depositing Ge onto catalyst sites. Evidence of this can be seen in the research conducted by Wang *et al.* who conducted growth of Ge nanowires under atmospheric pressure and at the lowest reported temperature, 275 °C. Their results showed that under these conditions, Ge nanowires grew along the <110> direction [12-14]. This same orientation was found by Hanrath and Korgel, who grew Ge nanowires at 20 MPa and 375 °C [5,18]. This process utilized a super critical fluid as a Ge source. The ultra-high pressure was required to maintain the highly volatile source in a liquid state.

In general, when a super critical fluid was used to grow Ge nanowires, the chamber pressure was extremely high, on the order of 10 MPa. For all other deposition methods, there is no discernable trend as to how the total pressure for the growth system was selected. Ge nanowire growth has been conducted both at and below atmospheric pressure as well using CVD, PLD, or PVD [6,8,9]. In most of these cases, the pressure was determined after the growth temperature was selected to ensure a sufficiently high deposition rate on the substrate. Because the deposition rate is proportional to the growth

rate of the nanowires, it can be said that the total internal pressure of the growth system has a direct effect on the growth rate of the nanowires. There is also no quantitative evidence to suggest that the total internal pressure of the growth system affects the crystallographic properties of the wires, such as crystallographic orientation or the relative number of defects present in individual wires. In the system used to conduct this investigation, it was found that Ge nanowires grown below atmospheric pressure had a higher growth rate than those grown at atmospheric pressure.

2.4.3 Substrate

The (111) crystallographic plane is the lowest energy, close packed plane for elements with the diamond cubic crystal structure. This is because it has the highest atomic packing density of any crystallographic plane in this crystal structure. Therefore, the <111> direction would be the lowest energy direction for axial growth, because it is normal to the (111) surface. It would seem reasonable to assume that a (111) diamond cubic substrate would improve the likelihood of growing Ge nanowires along the <111> direction. However, this theory does not always prevail. Nguyen *et al.* and Kammins *et al.* have reported vertical Ge nanowire growth on Ge(111) substrates and Si(111) substrates, respectively [11, 21]. These wires did grow along the <111> direction. <111> oriented Ge nanowires have also been grown on thermally grown amorphous SiO_2 and highly polished iron [12,15]. No orientation was specified for the Fe substrate. In addition to the <111> direction, these substrates also produced nanowires with the <110> and <112> directions.

There are theories as to why nanowires can grow in directions other than the <111> direction. Tan *et al.* developed a model for explaining the kinetics of growth along the <110> and <112> directions. They theorized that nanowires growing along each of these directions were predicated on a dislocation [22]. There is also speculation that a higher level of supersaturation of the alloy droplet leads to axial growth along the lowest energy direction, though the evidence to support such a theory is limited [18].

The literature suggests that substrate selection, like temperature and pressure, cannot definitely control the crystallographic properties of the nanowires. The thermodynamics of nanowire growth and defect formation appear to be the largest contributing factors in the axial orientation of the nanowires. Because the (111) plane has the highest packing density in the diamond cubic crystal structure, Ge nanowires are most likely going to grow in the <111> direction. This can be assisted by selecting a complementary substrate that has a diamond cubic crystal structure and is oriented in the <111> direction.

2.4.4 Catalyst

Catalysts are necessary for the VLS mechanism to take place. The catalyst in a VLS process is any metal that can alloy with the material desired to form a nanowire. For Ge nanowire and Si nanowire growth, the most common catalyst selected is gold. Both alloy easily with gold and exhibit eutectic behavior. The Au-Ge phase diagram and region of wire synthesis is shown in Figure 2. Though eutectic behavior is not necessary for nanowire synthesis, it allows for more accurate prediction of the behavior of the

system. Saturation of the catalyst is achieved when its composition reaches the liquidus composition in the binary system, resulting in wire growth. This is illustrated in Figure 2.

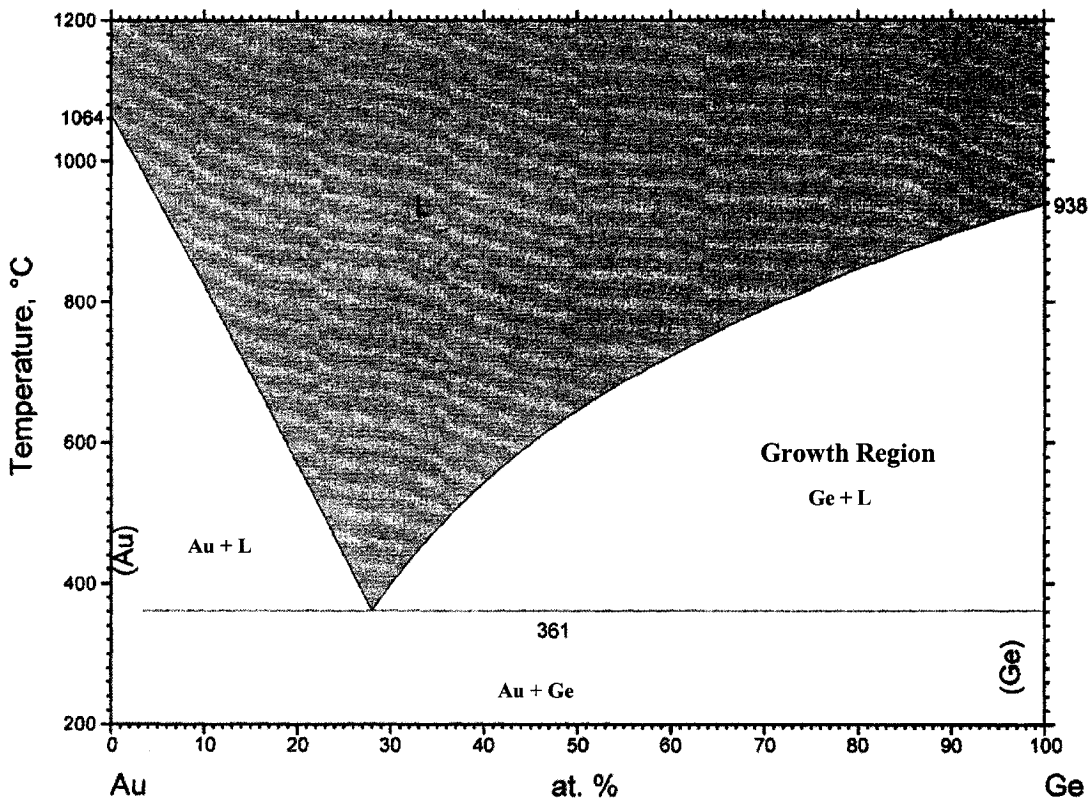

Figure 2. Au-Ge binary phase diagram. Reprinted with permission of ASM International®. All rights reserved. [23].

Other catalysts, such as Fe, have been used to grow nanowires [9]. Morales and Lieber utilized Pulsed Laser Deposition, which was discussed in section 2.2.2, to grow Fe catalyzed Ge nanowires. They used a 90% Ge 10% Fe target as their source material. The target was ablated with a laser and the vaporized material was collected on a cooled metal finger. The experiment was conducted in a heated chamber maintained at 820 °C. 90% Ge and 820 °C corresponds to a point in the two phase Ge(s) + $FeGe_2$(s) region on the Fe-Ge binary system, as shown in Figure 3. The relative quantities of the phases in a

sample with this composition will be 70% Ge and 30% $FeGe_2$, as calculated using the inverse lever rule. As the ablated material is collected on the cooled metal finger, it separates into the two distinct phases. This process produced Ge nanowires that were capped with $FeGe_2$ beads, which was confirmed with EDS [9].

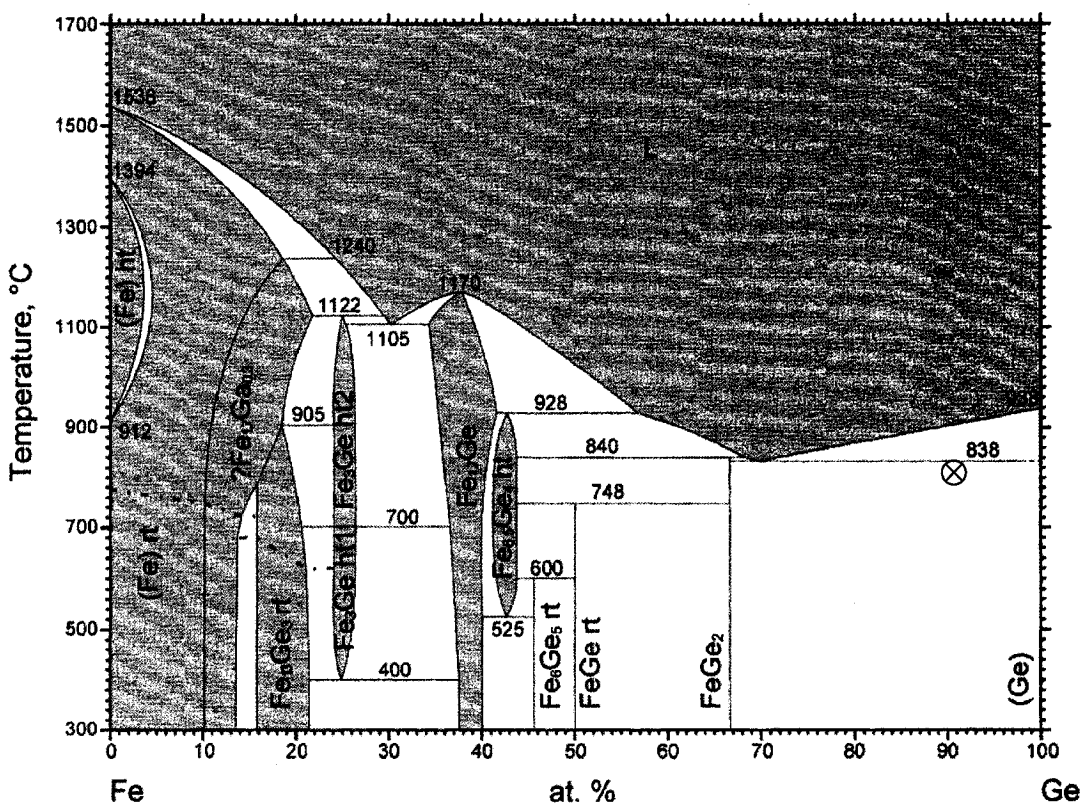

Figure 3. Fe-Ge binary phase diagram. Reprinted with permission of ASM International®. All rights reserved [24].

Catalyst selection is dependent on understanding the behavior of its interaction with the wire material. Theoretically, nanowires can be grown using almost any metal as a catalyst as long as the two materials exhibit a limited solid solubility. Once the catalyst droplet reaches saturation, the wire material will precipitate out. Having a lower solid

solubility of the catalyst material in the wire material will ensure a higher purity of the wire after growth.

2.5 Summary

Growth of Ge nanowires has been conducted using a variety of methods and conditions. There does not appear to be a well defined set of process parameters that can be identified as producing wires with the smallest concentration of defects. The crystallographic orientation of the wires is dependent on a host of conditions. The growth conditions themselves are dependent on the Ge deposition method. As previously stated, Wang *et al.* reported Ge nanowire growth at 275 °C and atmospheric pressure. They used germane as a source material. This process produced wires oriented along the <110> direction [12-14]. Arguably the most extreme conditions were used by Hanrath and Korgel. Their process was carried out at 375 °C and 20 MPa. This process also produced wires oriented along the <110> direction [5,18]. As can be seen from these two examples, the direction of axial growth in Ge nanowires can be difficult to predict.

Substrate selection may play a key role in increasing the probability of one orientation or another. A substrate of Si(111) should improve the chance of the growth process occurring epitaxially, producing wires with the <111> growth direction. However, Ge nanowires grown on amorphous surfaces, such as SiO_2, exhibit single crystalline growth in both the <110> and <111> directions. Furthermore, Ge nanowires grown on Fe grow in the <112> direction, though Ge has a different crystal structure and a lattice constant nearly twice as large as Fe.

It has been proposed that catalyst size can help determine orientation. Smaller catalysts reach saturation sooner than larger ones and therefore nucleate nanowires at a faster rate. This rate increase could force the wires to take a less energetically favorable orientation, such as the <110> direction.

With a variety of different processes and catalysts available, growth of Ge nanowires is not a difficult task. The growth conditions and results for various methods of Ge nanowire growth are summarized in Table 1. Controlling the location, axial growth direction, and orientation of wires with respect to the substrate appears to be a monumental task. Overcoming these challenges is desirable for incorporating nanowires into industrial applications.

In order for this next evolution in nanotechnology to progress, nanowire synthesis itself must be studied further. Without a more fundamental understanding of the parameters that control wire formation, bridging the gap between academic curiosity and useful technology for industry will be impossible.

Table 1. Summary of deposition methods and conditions for Ge nanowire growth.

Growth Method	Substrate Temperature	Source	Substrate	Catalyst	Xtal Orientation	Wire Diameter
CVD	275°C	GeH_4	SiO_2	Au nanocrystals, 20nm diameter	(110)	~23nm
CVD	310-425°C	GeH_4	Si(100), Si(111)	Au nanocrystals, 20nm diameter	(111)	40nm
SFLS	300-450°C	$(CH_3CH_2)_4Ge$ or $(C_6H_5)_2H_2Ge$	Si(100)	Au nanocrystals, 2.5-6.5 nm diameter	(111), (110)	10-150nm
PVD	500°C	Ge Powder	Si	2 nm Au thin film	(111)	20-180nm
PVD	500°C	Ge Powder	SiO_2	10 nm diameter Au nanoparticles	(111)	20-45nm
SFLS	600°C	Diphenylgermane	Alumina-MTF	na	(100)	2-5nm
PLD	820°C	$Ge_{0.9}$-$Fe_{0.1}$ Target	Cold Finger	Self Seeding	(110)	3-9nm
PVD	800-1000°C	Ge+GeI_4 Powder	Si(001)	50-200Å Au	(111), (220), (311)	5-300nm

CHAPTER THREE

OBJECTIVES

Single crystal semiconductor nanowires are of interest because they may be used in the fabrication of nano-electronics, such as next generation transistors. Ge nanowires have been fabricated using Au and Fe as catalysts. Neither of these catalysts is ideal for device fabrication, either because they can be contaminants or do not enhance the properties of the nanowire after growth. Growth of nanowires using industry friendly catalysts such as indium (In) or antimony (Sb) will allow for easier integration of nanowires into the semiconductor industry. In and Sb are also commonly used as dopants in semiconductors. Based upon the binary phase diagrams of the Ge-In and Ge-Sb systems, it was theorized that Ge nanowire growth would be possible with either of these two metals (In and Sb) as catalysts. Both metals exhibit binary eutectic behavior with Ge. The binary eutectic point in both systems is close to 100% In and Sb, respectively. These features can be seen in Figure 4 and Figure 5. The lack of stoichiometric compounds in either system also made them ideal candidates for precipitation of nearly pure Ge. The maximum solid solubility of In in Ge is 0.122 atomic percent [25]. The maximum solid solubility of Sb in Ge is 0.0715 atomic percent [25]. This study was undertaken to determine if by varying the thickness of the catalyst and the growth temperature, growth of nanowires with varying diameters could be grown.

There were two primary objectives of this study. The first objective was to study the deposition and growth of Ge on Si and SiO_2 substrates, coated with In films between

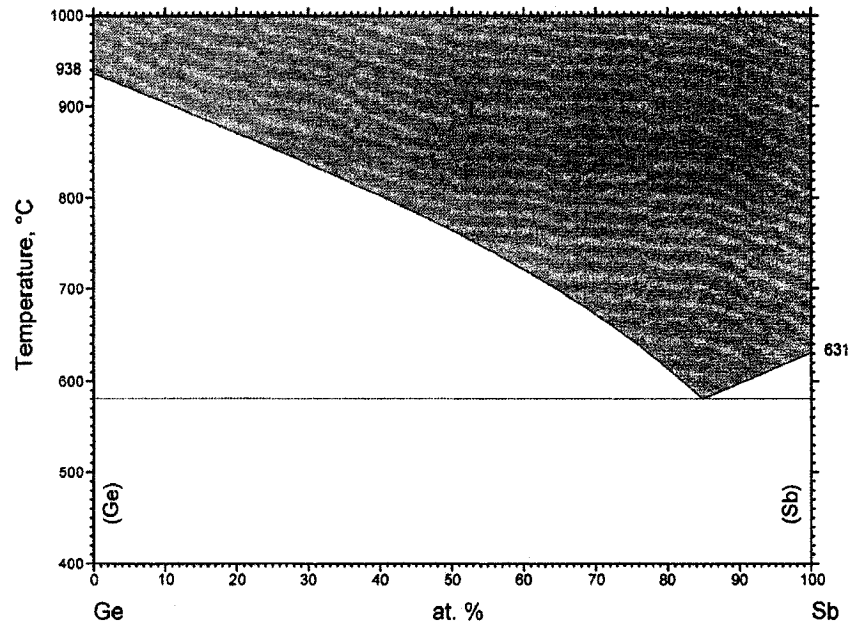

Figure 4. Ge-Sb binary phase diagram. Reprinted with permission of ASM International®. All rights reserved [26].

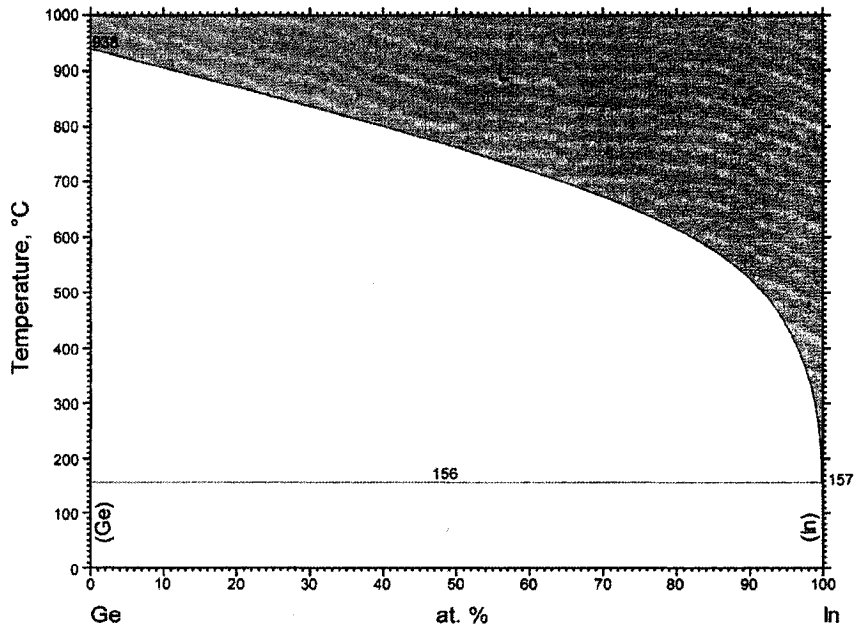

Figure 5. Ge-In binary phase diagram. Reprinted with permission of ASM International®. All rights reserved [27].

1 nm and 30 nm thick, at temperatures between and including 100 °C and 600 °C. The second objective of this research was to study the deposition and growth of Ge on Si and SiO_2 substrates, coated with Sb films between 1 nm and 10 nm thick, at temperatures between and including 560 °C and 700 °C.

The secondary set of objectives, contingent on whether or not nanowires were present on the surface of the substrates following Ge deposition, was to characterize the process and the nanowires. If nanowires were present on any of the substrates after Ge deposition, density of these wires on the surface was measured from scanning electron microscope images. Further, if these nanowires could be removed from their substrates and dispersed onto a transmission electron microscope grid, their diameters were measured and the crystallographic direction they were growing in was determined.

CHAPTER FOUR

EXPERIMENTAL METHODOLOGY

4.1 Introduction

As discussed in Chapter 3, the deposition of Ge on In and Sb-coated substrates was studied. Before the substrates could be processed, they had to be coated with thin films of the catalyst metals. Prior to the deposition of In and Sb films, the substrates were cleaned washing in acetone to dissolve and remove any residual organic films. This was followed by soaking in methanol to remove any remaining acetone. After this, the substrates were soaked in isopropanol to remove any remaining methanol. The substrates were then rinsed in deionized water to remove any remaining solvents. This procedure is the same used for cleaning metal tweezers at the Stanford Nanofabrication Laboratory. The Si(111) substrates were then washed in an aqueous hydrofluoric acid solution to remove any native oxide, followed by a rinse in deionized water.

After being cleaned, the substrates were placed directly into the sputter chamber for the deposition of the catalyst metals. The sputtering process was conducted at 10^{-6} torr. After the catalyst films had been deposited, the substrates were placed into the process chamber for Ge deposition. For Sb, a range of temperatures were selected above and below its melting point, 650 °C. The thicknesses of the films used in the Sb-catalyst study were selected based on of previous experiments with Au-catalyzed Ge nanowire growth in the same experimental system.

Germanium deposition on In-coated substrates occurred in three stages. Initial experiments with In-coated substrates were conducted at temperatures around the melting

temperature of In, 150 °C, and with film thicknesses used in previous experiments with Au-catalyzed Ge nanowire growth in the same experimental system. This initial set of experimental parameters yielded no nanowire growth on the substrates. In addition, no Ge deposition could be found on the substrates. Because the quartz tube was becoming opaque much more quickly with these parameters than with experiments conducted at higher temperatures, it was thought that the majority of the vaporized Ge was depositing on the walls of the tube before it could reach the substrate.

To compensate for this, a new exploratory experiment was designed, based on temperatures that had been used to successfully grow Au-catalyzed Ge nanowires, with growth temperatures of 400 °C and 450 °C. The substrates were again coated with films ranging from 1 nm to 10 nm of In. These temperatures yielded sporadic growth on substrates with 10 nm of In. From these observations, a new set of experiments was designed with growth temperatures ranging from 400 °C to 600 °C, and with catalyst films ranging in thickness from 10 nm to 30 nm of In.

Following Ge deposition, the substrates were examined using a scanning electron microscope (SEM) to determine if there were any nanowires present. If there were nanowires, three separate images were taken from different locations on the substrate for surface density calculations. Following SEM analysis, the wires on the substrates were transferred to SiO coated transmission electron microscope (TEM) grids. TEM images were used to calculate the average diameter of the In-catalyzed Ge nanowires as well as verify the crystallographic direction of the long axis of the wires and the lattice spacing

of the wires. When available, both EDS and electron diffraction patterns were taken of the nanowires. Figure 6 is a flow chart of the complete experimental procedure.

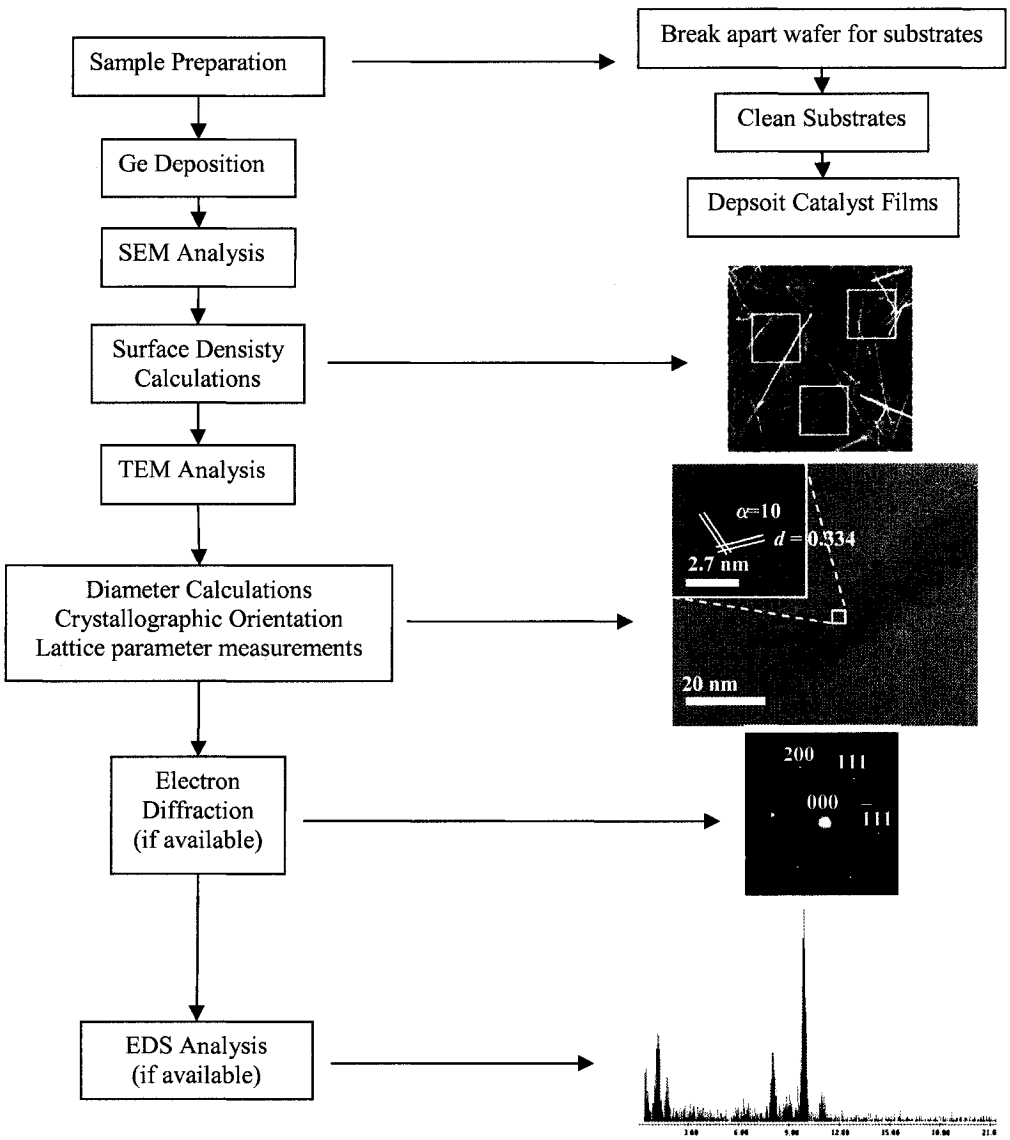

Figure 6. Experimental procedure used to grow and characterize In and Sb-catalyzed Ge nanowires.

4.2 Experimental Materials

The gases used to transport the vaporized Ge to the substrates for nanowire growth were ultra high purity argon, Ar, and hydrogen, H_2. The Ar was selected to carry the vaporized Ge to the substrates. The H_2 was selected to act as a reducer to prevent or minimize the formation of GeO_2 on the Ge nanowires. The Ge source material was a mixture of high purity Ge powder and high purity carbon graphite powder in a 1:1 weight percent ratio. The carbon graphite powder was used to prevent the Ge powder from agglomerating into a solid mass, which would cause the flow of vaporized Ge to decrease because of the loss of surface area. The specific details for the gases and raw materials used for this study are summarized in Table 2.

Table 2. Experimental materials for Ge nanowire growth.

Species	Purity	Manufacturer	Flow Rate	Size
H_2	99.999%	Scott Specialty Gas	70 sccm	
Ar	99.999%	Scott Specialty Gas	140 sccm	
Ge	99.99%	Alfa Aesar		100 mesh
C(Graphite Powder)	99.9%	Alfa Aesar		250 mesh

The ratio of the gas flow rates as well as the ratio of the powder source materials was selected from conditions used in previous experiments that yielded favorable Ge nanowire growth with Au coated substrates in the same experimental system.

4.3 Experimental Equipment

The experimental system used to grow Ge nanowires in this study consisted of two components: the growth reactor and the delivery system. The delivery system refers to the equipment used to deliver and control the flow of the Ar and H_2 into the growth reactor. The Ar and H_2 were independently transported through 0.5 in. diameter Tygon R-3606 laboratory tubing to two separate MKS Mass Flo controllers. The controllers were individually calibrated for Ar and H_2 and were used to regulate the flows of the gases to the growth reactor. After passing through Mass Flo controllers, the gas lines were combined and connected to the growth reactor.

The growth reactor consisted of a 1" x 48" quartz tube and two identical Lindberg Blue M Mini Mite tube furnaces, model number TF55035A. The maximum temperature the furnaces were capable of was 1100 °C. The furnaces were used to independently heat the substrates and the source material. The quartz tube was laid across the center channel of the tube furnaces. This system is illustrated schematically in Figure 7.

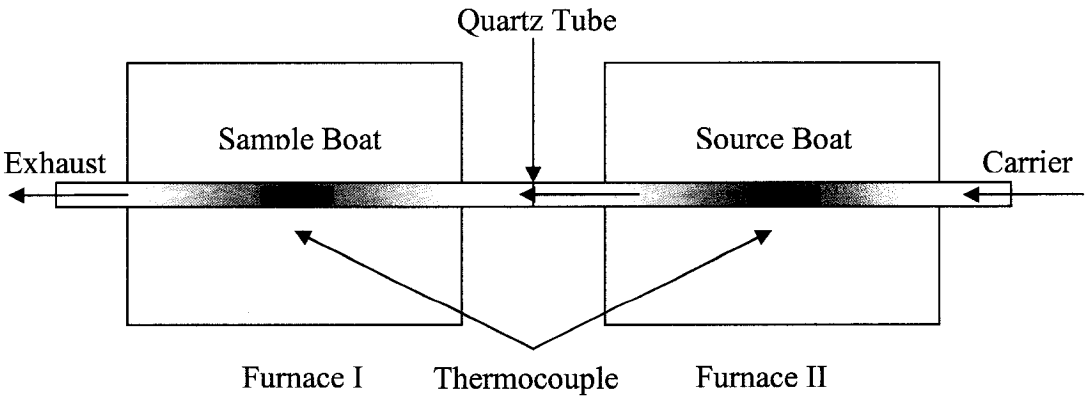

Figure 7. Experimental setup for nanowires growth.

The temperature of both the substrate furnace and the source furnace was measured by a thermocouple located at the mid point along the length of the tube trough. The furnaces were separated by a distance of 3" to ensure the furnaces were thermally isolated from each other. To ensure accurate temperature control for the experiment, the boats carrying both the specimens and source material were centered in their respective furnace, corresponding to the location of the thermocouples.

4.4 Experimental Procedure

The following sections describe the complete procedure used in this study for growing and characterizing In and Sb-catalyzed Ge nanowires.

4.4.1 Sample Preparation

The substrates used for Ge nanowire growth were n-type Si(111) with a 4° off normal orientation and n-type Si(001) with a 400 nm thick layer of thermally grown SiO_2. Si(111) was chosen as the substrate because both silicon and germanium have diamond cubic crystal structures with a difference in lattice parameters of 0.023 nm. Also, the (111) orientation has the highest atomic packing density, which is expected promote epitaxial growth in the nanowire. The SiO_2 substrate was selected because device fabrication would be easier on an insulating surface. Prior to growth all substrates were prepared by removing any organic residues and any native oxide layers. The process was as follows:

1. Break wafers into ~1 cm^2 pieces.
2. Clean wafer fragments individually in acetone using ultrasonic agitation to remove any organic films.
3. Clean wafer fragments individually in methanol using ultrasonic agitation to remove any residual organic films or acetone.
4. Clean wafer fragments individually in isopropanol using ultrasonic agitation to remove any residual organic films or methanol.
5. Rinse wafer fragments in double distilled water to remove any residual isopropanol.
6. Soak the Si(111) wafer fragments in 10% HF for five minutes to remove any native oxide layer.
7. Rinse twice with double distilled water and air dry with N_2.
8. Immediately use an ion beam sputterer to deposit films of Sb and In onto specimens.

4.4.2 Ge Deposition

After the specimens had been coated with their respective catalyst films, they were placed on top of a quartz boat and loaded into the tube furnace. In-coated specimens were processed at different times than Sb-coated specimens. Si and SiO_2 specimens that were coated with the same amount of catalyst were positioned next to each other across the diameter of the quartz tube. The specimens were arranged sequentially according to the thickness of their catalyst films. The specimens with the thinnest films were placed upstream in the quartz boat, closest to the source material. Specimens with successively thicker films were placed further downstream in the quartz

boat. After the quartz boat was loaded with specimens, it was placed into the quartz tube and positioned over the thermocouple in the growth reactor. The boat containing the source material was then loaded into the quartz tube and positioned over the thermocouple in the source furnace.

The complete range of temperatures and catalyst thicknesses for In-coated substrates that were experimented with is shown in Table 3. The initial catalyst thicknesses selected were chosen because of past experiments conducted with this system on Au-catalyzed Ge nanowire growth. The initial temperatures selected were predicated on the eutectic temperature of the Ge-In system, 156.6 °C.

After an initial round of experiments with In-coated specimens yielded no Ge deposition on the substrate, the experiment was repeated at temperatures that had produced Au-catalyzed Ge nanowires with this system. The two initial experiments at 400 °C and 450 °C yielded only sporadic patches of nanowires on the specimens coated with 10 nm of In. A third experiment was conducted at temperatures between 400 °C and 600 °C with specimens coated with In films between 10 nm and 30 nm thick.

Table 3. Experimental matrix for In-coated substrates.

	Growth Temperature (°C)									
Catalyst Thickness (nm)	100	150	200	400	425	450	475	500	550	600
1	In	In	In	In		In				
2	In	In	In	In		In				
4	In	In	In	In		In				
6	In	In	In	In		In				
10	In	In	In	In	In	In	In	In	In	In
15				In	In	In	In	In	In	In
20				In	In	In	In	In	In	In
25				In	In	In	In	In	In	In
30				In	In	In	In	In	In	In

The complete range of temperatures and catalyst thicknesses for Sb-coated substrates that were experimented with is shown in Table 4. The catalyst thicknesses selected were also based on past experiments conducted with this system on Au-catalyzed Ge nanowire growth. The temperatures selected were predicated on the melting temperature of Sb, 630.6 °C. This differs from the selection criteria for In-coated substrates because the melting temperature for In, 156.6 °C, and the eutectic temperature for the Ge-In system, 156 °C, are nearly identical.

Table 4. Experimental matrix for Sb-coated substrates.

	Growth Temperature (°C)					
Catalyst Thickness (nm)	560	610	630	650	670	700
1	Sb	Sb	Sb	Sb	Sb	Sb
2	Sb	Sb	Sb	Sb	Sb	Sb
4	Sb	Sb	Sb	Sb	Sb	Sb
6	Sb	Sb	Sb	Sb	Sb	Sb
10	Sb	Sb	Sb	Sb	Sb	Sb

The temperature profile for the growth process included four stages (I-IV). Stage I was a pre-growth purge of the reactor tube with a constant flow of 140 sccm of Ar and 70 sccm of H_2. This was conducted at room temperature. Following the purge, the furnace temperature was then increased during Stage II to the growth temperature. Stage III began when the furnace had reached the growth temperature. The temperature was held constant at this temperature for the desired growth duration. The furnace was then cooled to room temperature during Stage IV. This process is illustrated in Figure 8.

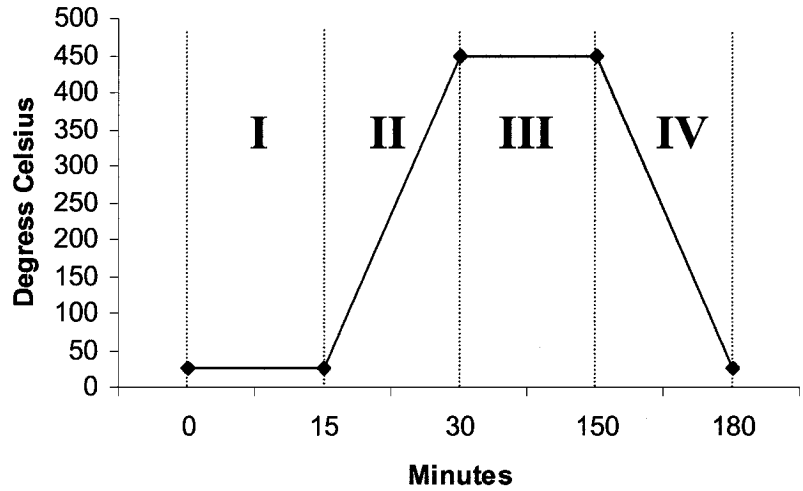

Figure 8. Temperature heating profile for In-catalyzed Ge nanowire growth.

4.4.3 Data Collection and Analysis

Specimens were first examined to determine whether or not there was any nanowire growth. This was conducted using a Hitachi S-4000 field emission scanning electron microscope (SEM) operated with an accelerating voltage of 30 keV. If wires were present, their surface density and diameters were measured and the crystallographic direction they grew in was determined. The surface density was evaluated because it would be an indicator of how many wires would be available to conduct device studies on. The wire diameter is directly related to any quantum confinement effects that would be seen in the wires. The crystallographic orientation is important because different orientations have different electron and hole mobility.

From each specimen with nanowires present on it, the number of wires present in three separate 5 μm^2 regions per specimen was used to determine the mean and standard deviation of the Sb-catalyzed Ge nanowire surface density. Because of the higher surface

density of Ge nanowires found on the In-coated substrates, nine separate 0.25 μm^2 regions per specimen were used to determine the mean and standard deviation. However, In-catalyzed Ge nanowires were only successfully grown on one SiO_2 substrate and one Si(111). All data in Chapter 5 are based upon these two specimens.

A Philips CM20 field emission gun transmission electron microscope (TEM), operated at 200 keV and equipped with EDAX, was used to measure the average diameter and lattice parameter of the nanowires. In addition, TEM images were used to determine the crystal structure of the nanowires and crystallographic direction the wires were growing in. If possible, an electron diffraction pattern was obtained to corroborate both the crystal structure of the nanowires and the crystallographic direction they were growing in. When the EDAX detector was operating, EDS measurements were taken of the wires for compositional analysis.

CHAPTER FIVE

RESULTS

All SEM, TEM, EDS and electron diffraction data available for In and Sb-catalyzed Ge nanowires that were grown in this study are presented in this chapter. From SEM data, the mean surface density of both In-catalyzed and Sb-catalyzed Ge nanowires wires was calculated. The atomic lattice spacing, crystal structure, and the crystallographic direction of growth of both types of Ge nanowires were calculated from TEM data. In addition, the mean diameter of the In-catalyzed Ge nanowires was also calculated from TEM data. EDS data was used to confirm the composition of the In-catalyzed Ge nanowires. The composition of the Sb-catalyzed Ge nanowires was inferred from the lattice parameter measurements and electron diffraction patterns.

5.1 In-Catalyzed Ge nanowire Growth

In-catalyzed Ge nanowires were successfully grown once on both Si and SiO_2 substrates at 450 °C when the In films were thicker than 25 nm, as seen in Table 5. The nanowires that were grown at 450 °C were found to have relatively few defects along their lengths, in addition to growing in relatively high densities, based on SEM analysis. It was also found that multiple types of structures grew across the surface; these could not be classified as nanowires but did appear to grow via the VLS mechanism.

Table 5. Experimental matrix for In-coated substrates with location of successful growth highlighted.

Catalyst Thickness (nm)	Growth Temperature (°C)									
	100	150	200	400	425	450	475	500	550	600
1	In	In	In	In		In				
2	In	In	In	In		In				
4	In	In	In	In		In				
6	In	In	In	In		In				
10	In	In	In	In	In	In	In	In	In	In
15				In	In	In	In	In	In	In
20				In	In	In	In	In	In	In
25				In	In	In	In	In	In	In
30				In	In	In	In	In	In	In

The wires grown at 450 °C grew along both the <111> and <112> directions, as found using TEM analysis. Measurement of the inter-planar spacing of the wires agreed with published data regarding the lattice constant of elemental germanium, 0.5656 nm. EDS analysis of the wires confirmed their composition as being Ge, as shown in Figure 9. The Si, O, C, and Cu peaks are the from the TEM grid.

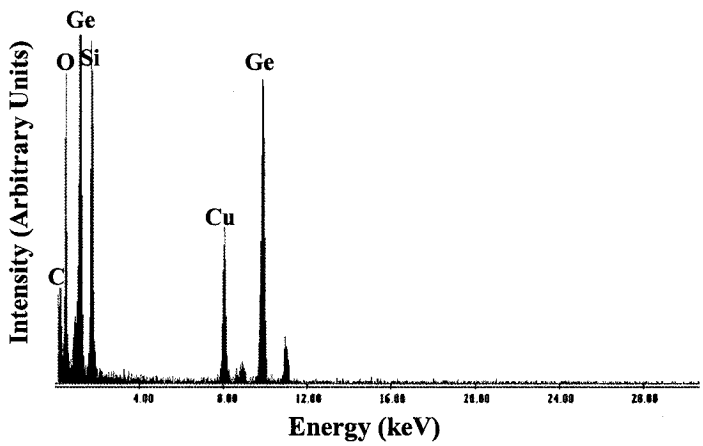

Figure 9. EDS spectrum taken from a single In-catalyzed Ge nanowire.

5.1.1 Morphology and Surface Density

The morphology of the wires was affected most significantly by changes in growth temperature. At lower growth temperatures, *e.g.* 400 °C, structures were sporadically found across the surface. However, these structures could not be classified as nanowires. The structures had irregular shapes with non-uniform diameters along their length. Figure 10a is an example of one of these structures. Also found at this temperature were nanowires that were extremely short and had extremely thin diameters. The length of the wires was approximately 500 nm. The diameters were too thin to measure accurately with the resolution of the SEM used in this study. This is shown in Figure 10b. These nanowires grew in sporadic colonies across the substrate. Figure 10c is a wider field view of one of these colonies. It is not known if these two structures grew through the VLS process. At 425 °C, nanowire growth was observed in relatively low surface densities along with structures that were similar to those found on substrates processed at 400 °C. The nanowires found at this temperature were approximately 1 μm in length and had irregular shapes, making them unusable for device study applications. These are seen in Figure 10c and 10d. A semispherical cap at the end of these structures indicated that they were grown through the VLS process. With catalyst thicknesses above 20 nm, the length of structures found across the surface decreased significantly. At this stage, the structures could again no longer be classified as nanowires because their length and diameters were nearly the same, approximately 500 nm. The structures still appeared to grow by the VLS mechanism due to the presence of spherical caps on their ends, as seen in Figure 10f.

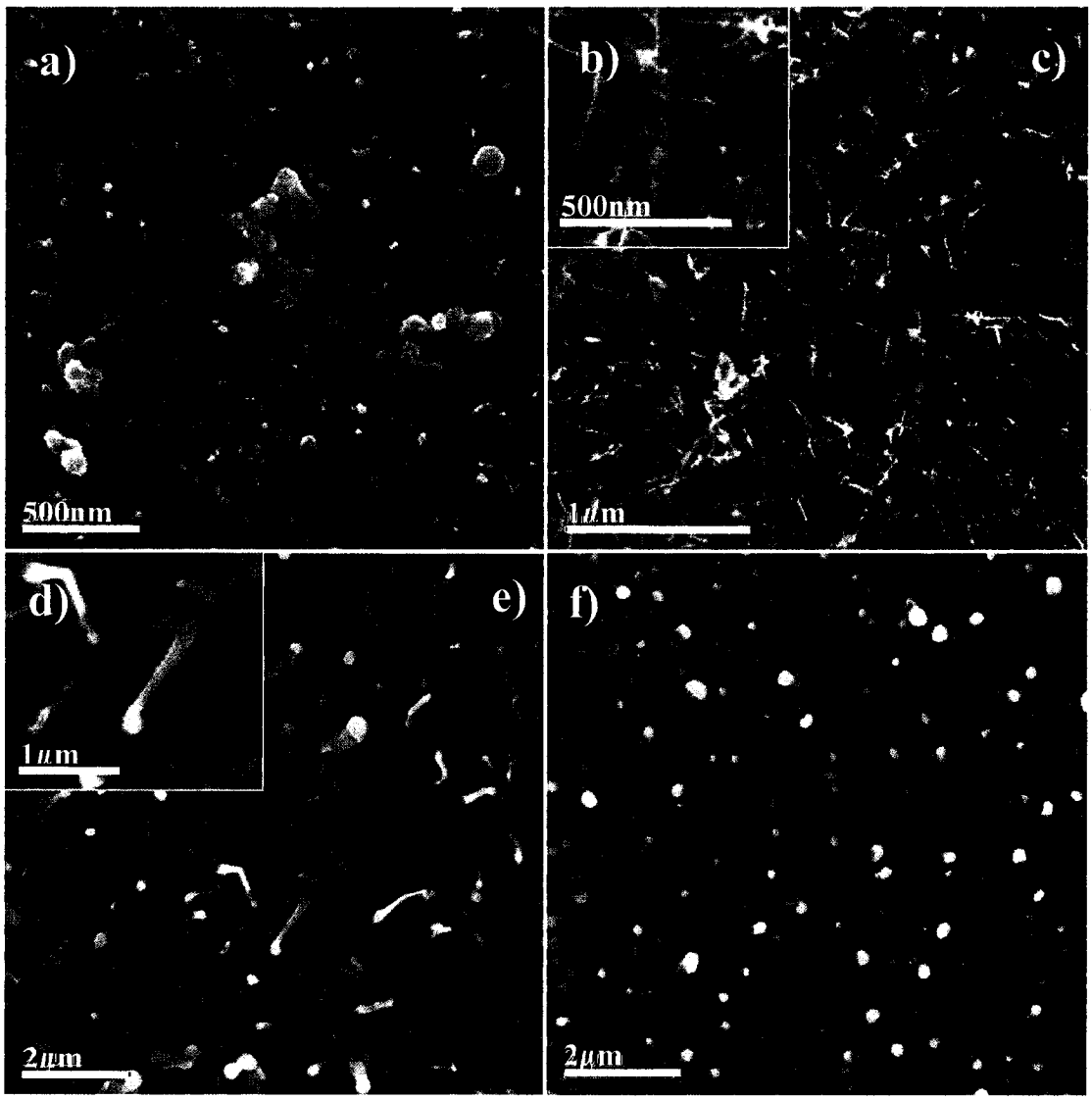

Figure 10. a) Ge nanostructures grown at 400 °C on SiO_2 coated with 25 nm of In b) Ge nanowire colony grown at 400 °C on Si(111) coated with 30 nm of In c) Ge nanostructures grown at 425 °C on SiO_2 coated with 25 nm of In d) Ge nanostructures grown at 425 °C on Si(111) coated with 25 nm of In.

Nanowires in significant quantities were found on both SiO_2 and Si(111) substrates processed at 450 °C with catalyst film thicknesses greater than 25 nm. The wires grew with high surface densities and lengths in excess of several microns. The

nanowires grew in higher densities on specimens with thicker catalyst films. The surface density of nanowires grown on SiO_2 was nearly double that of nanowires grown on Si(111), as shown in Table 6.

Table 6. Surface densities in μm^{-2} for In-catalyzed Ge nanowires.

Catalyst Thickness(nm)	SiO2	Si(111)
30	28.5	14.79

SEM images show the wires grown on both substrates have few obvious defects along their length, as seen in Figures 11a and 11b. In addition to the wires, there were also sporadic structures that were much larger than nanowires, though they appeared to grow through the VLS mechanism due to the spherical cap at their end. Figures 11c and 11d are SEM images of one of these structures that is up to a micron in diameter and tens of microns in length. No nanowires were found on specimens that had been coated with less than 30 nm of In. At 475 °C, almost no nanowires were found on any specimens. The substrates instead had a large quantity of the extremely large pillar like structures found in small numbers on specimens processed at 450 °C. The structures typically had a significant taper from bottom to tip, indicating three dimensional growth was taking place. The structures often had a semispherical cap at their free end. This would, again, suggest that the structures are growing through the VLS mechanism. Most of the structures possessed at least one significant defect along their length. In addition, some of the structures had nanowires sprouting from their tips, as seen in Figure 12.

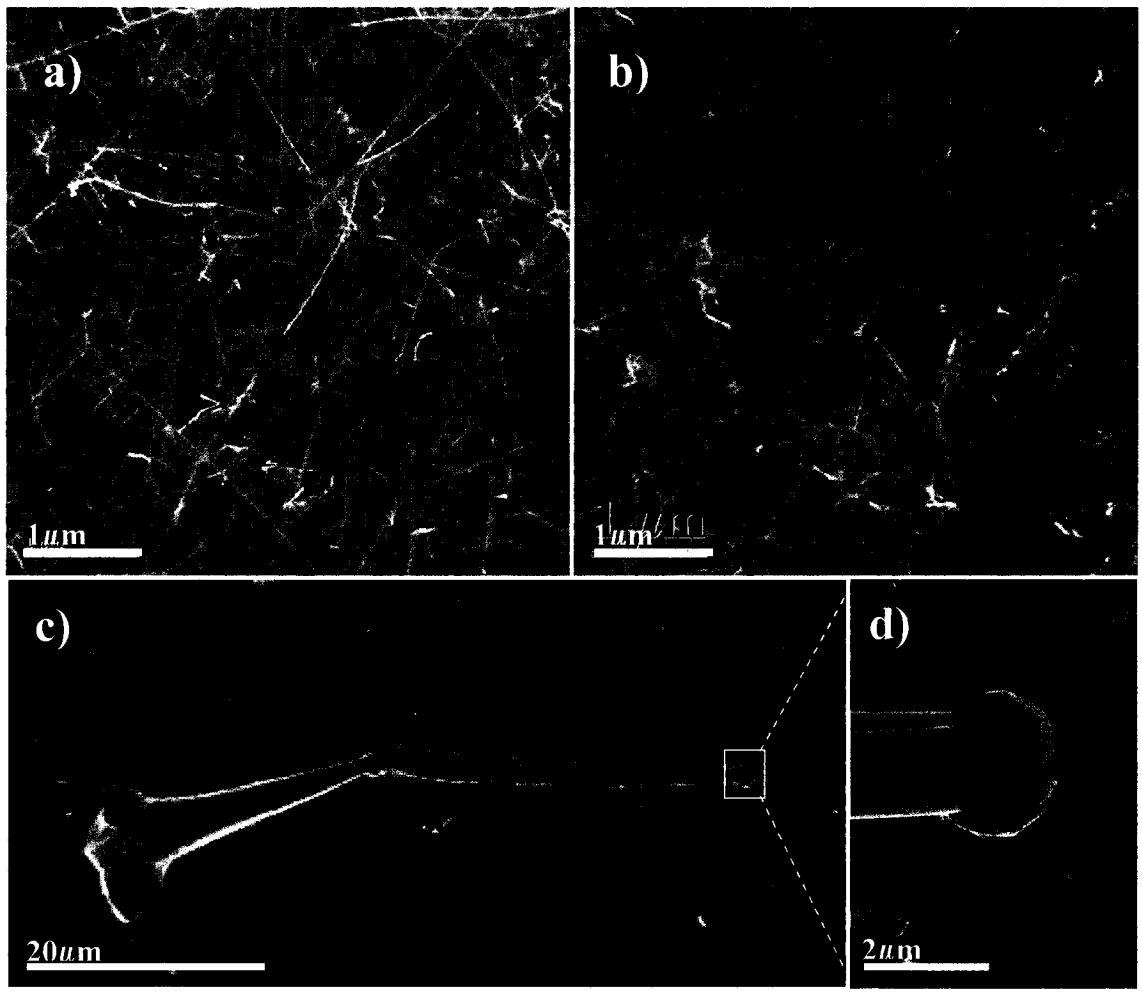

Figure 11. a)Ge nanowires grown at 450 °C on SiO_2 coated with 30 nm of In b) Ge nanowires grown at 450 °C on Si(111) with 30 nm of In c) Ge whisker grown at 450 °C on Si(111) coated with 25 nm of In d) Tip of Ge whisker.

At 500 °C, the specimens were covered in smaller versions of the structures found at 475 °C. The structures all had a strong taper from their base and end in a very long and very thin nanowire. Above 500 °C, no such structures are found. The substrates were typically covered in particles and debris, which were thought to be Ge or GeO_2.

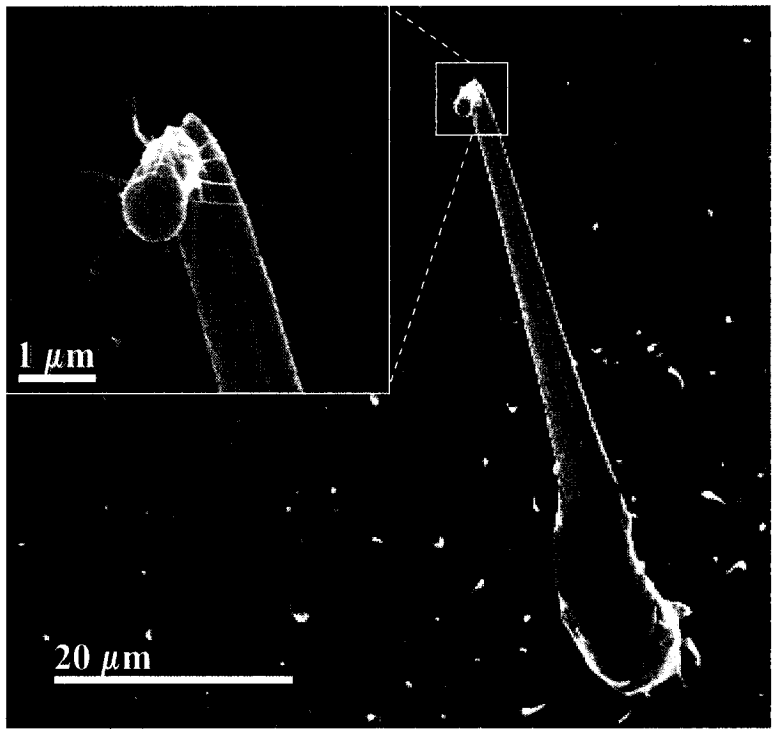

Figure 12. Ge whisker with Ge nanowires sprouting from its tip.

In summary, lower growth temperatures, 400 °C and 425 °C, produced structures that could not be classified as nanowires because of their irregular shapes or because the ratio of their length to their diameter was too close to 1. At 450 °C, nanowires were grown in high densities with uniform diameters along their length. These nanowires were also multiple microns in length. Above 450 °C, any structures found on the substrate exhibited tapered diameters as well as diameters and lengths that made them too large to be classified as a nanowire. Though these structures appeared to grow via the VLS mechanism due to the presence of spherical catalyst tips, their tapered diameters

indicated that they were also growing three dimensionally. Above 500 °C, there was no evidence of VLS growth of any kind.

5.1.2 Compositional and Crystallographic Analysis

Crystallographic analyses, mean diameter measurements, and compositional analysis of the Ge nanowires were performed with a Philips CM20 HRTEM operated at 200 keV and equipped with an EDS detector. Only fifteen nanowires grown on Si(111) and twelve nanowires grown on SiO_2 were able to be isolated under the electron beam of the TEM. The diameters of the fifteen nanowires grown on Si(111) and the twelve nanowires grown on SiO_2 were measured. The average diameter of the nanowires grown on Si(111) was found to be 14.9 nm with a standard deviation of 4.4 nm. The nanowires grown on SiO_2 had an average diameter of 15.0 nm with a standard deviation of 2.6 nm.

Lattice fringes were visible on twelve of the fifteen nanowires grown on Si(111) and all twelve of the nanowires grown on SiO_2. Of the nanowires grown on Si(111), HRTEM images showed that ten were growing along the <111> direction. The images of the remaining two nanowires showed the close packed planes running parallel to the direction of growth of the nanowires. Though no electron diffraction data were available, previous research conducted by Mathur *et al.* showed wires with similar crystallographic planes grew along the <112> direction [15]. Figures 13a thru 13e are HRTEM images of In-catalyzed Ge nanowires grown on SiO_2 and Si(111). The images show the Ge nanowires are single crystals and contain no noticeable defects, such as dislocations or stacking faults. The lattice spacing of 0.33 nm corresponds to a lattice constant of 0.572

nm, which is consistent with the published value of the lattice constant of elemental Ge, 0.5658 nm [23]. The angle between two sets of (111) planes was measured at 109.5°, which is consistent with the difference between intersecting (111) planes of a diamond

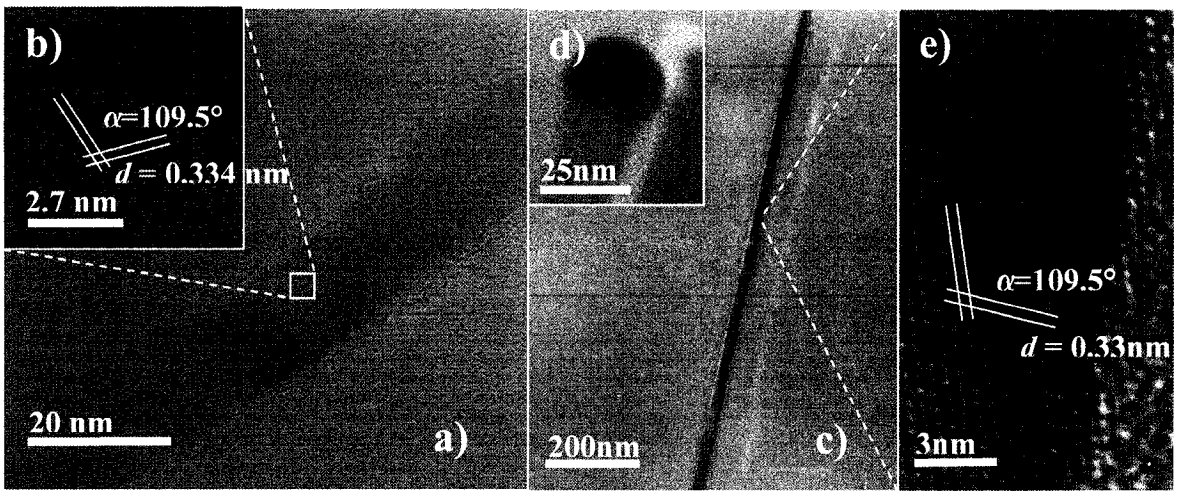

Figure 13. a) HRTEM image of an In-catalyzed Ge nanowire grown on SiO_2
b) HRTEM image of nanowire in 11a with visible intersecting (111) lattice planes and measurements c) HRTEM image of an In-catalyzed Ge nanowire grown on grown on Si(111) d) catalyst tip of the nanowire in 11c e) HRTEM image of nanowire in 11c with intersecting (111) planes and measurements.

cubic crystal structure [28]. Calculations for determining the distance and angle between planes are included in Appendices A and B, respectively. The orientation of the (111) plane with respect to the growth axis indicates that the Ge nanowires grew preferentially along the <111> direction.

The composition of the nanowires was determined with EDS. Figure 14 is an EDS spectrum taken from the tip of the nanowire in Figure 13d. Only Ge and In were detected, which further confirms the In bead on the wire tip leading the Ge nanowire growth, following the VLS mechanism. The blue spectrum in Figure 14 is from the

TEM grid itself, explaining the presence of Si, O, C, and Cu in the measurement of the nanowire.

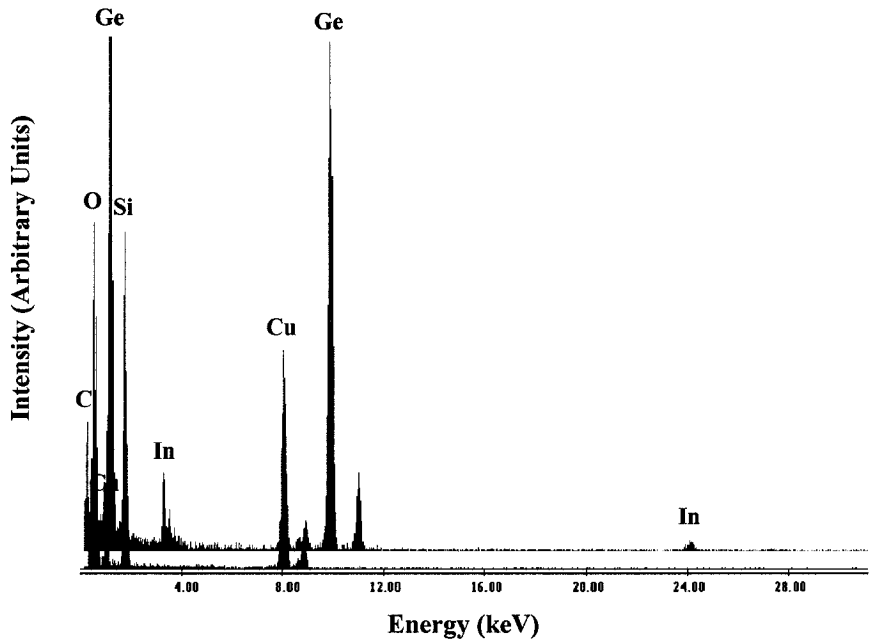

Figure 14. EDS spectrum taken from the junction of the nanowire and catalyst tip in Figure 11d. The lower spectrum in blue is an EDS spectrum taken from the TEM grid itself.

5.2 Sb-catalyzed Ge nanowire growth

Sb-catalyzed Ge nanowires were successfully grown on SiO_2 substrates with Sb films between 4-10 nm thick and processed at temperatures between 630 °C and 670 °C. Table 7 shows the temperatures where Ge nanowire growth was successful. SEM analysis of Sb-coated SiO_2 substrates showed nanowires with a unique morphology resembling a string of pearls. No nanowires grew on Sb-coated Si substrates.

Table 7. Experimental matrix for Sb-coated substrates with location of successful growth highlighted.

Catalyst Thickness (nm)	Growth Temperature (°C)					
	560	610	630	650	670	700
1	Sb	Sb	Sb	Sb	Sb	Sb
2	Sb	Sb	Sb	Sb	Sb	Sb
4	Sb	Sb	Sb	Sb	Sb	Sb
6	Sb	Sb	Sb	Sb	Sb	Sb
10	Sb	Sb	Sb	Sb	Sb	Sb

TEM analysis of the nanowires showed that they had grown along the <111> direction. Measurement of the inter-planar spacing in the wires agreed with published data for the lattice constant of elemental Ge. Electron diffraction patterns taken from the nanowires confirmed they were diamond cubic. From this information, it is reasonable to state that in this study, Sb-catalyzed Ge nanowires were successfully grown.

5.2.1 Morphology and Surface Density

As stated in section 5.2, the Sb-catalyzed Ge nanowires grew with a beaded morphology resembling a string of pearls. Figure 15 is a collection of SEM images taken from various specimens. The individual beads were not uniformly shaped or spaced along the length of an individual wire. This made determining an average diameter of these nanowires impossible.

The surface density of the nanowires was affected by changes in temperature and catalyst thickness. Figure 16 is a graph of the average surface densities of Sb-catalyzed

Ge nanowires with different catalyst thicknesses and processed between 610 °C and 670 °C. The highest average surface density observed, 2.76 μm^{-2}, was recorded on SiO_2

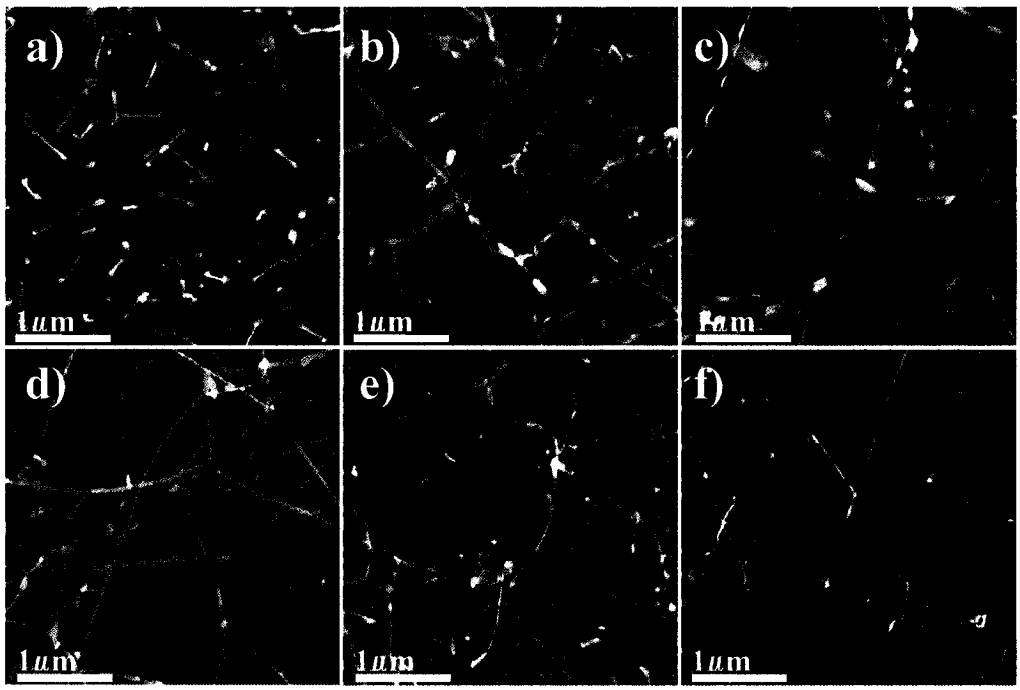

Figure 15. Sb-catalyzed Ge nanowires grown at various process conditions. a) 10 nm at 650 °C b) 6 nm at 630 °C c) 6 nm at 670 °C d) 4 nm at 650 °C e) 10 nm at 610 °C f) 10 nm at 670 °C.

substrates that had been coated with 4 nm of Sb and processed at 650 °C. The next highest surface density, 2.53 μm^{-2}, was recorded on SiO_2 substrates that had been coated with 10 nm of Sb and processed at 610 °C. This sample also had the highest recorded standard deviation at 2.94 μm^{-2}, which is higher than the calculated average. At 670 °C, the surface density dropped significantly, with the lowest surface density recorded at 0.46 μm^{-2} on SiO_2 that had been coated with 6 nm of Sb. Above and below the growth range, no structures were found across the substrate except for particle deposits. It was speculated that these were GeO_2.

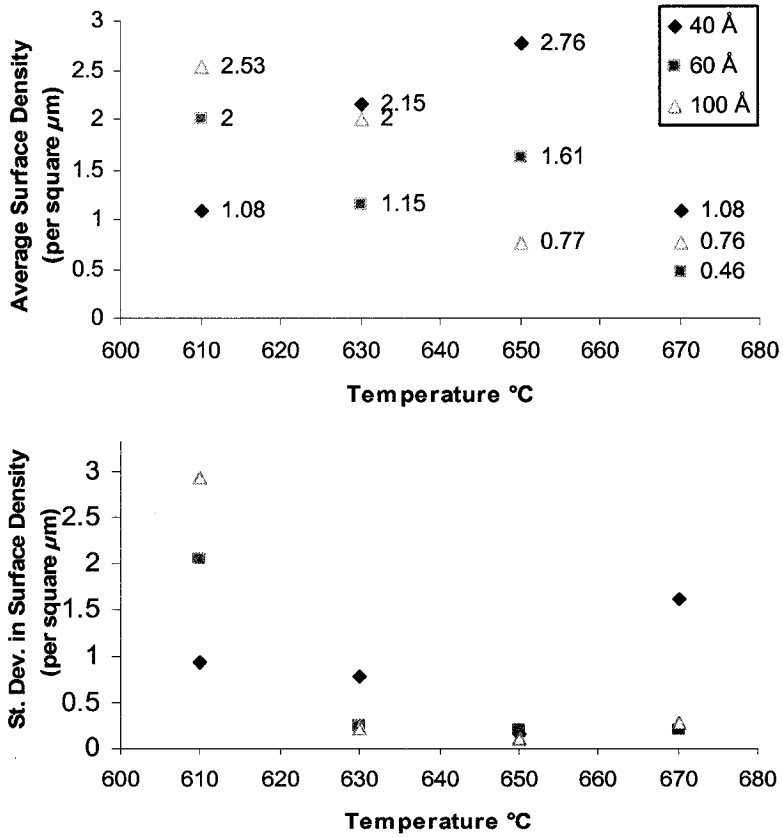

Figure 16. Average surface densities as measured across all samples where Sb-catalyzed Ge nanowires were grown. The lower chart shows the standard deviation in the average measurements.

5.2.2 Compositional and Crystallographic Analysis

The crystallography of the nanowires was investigated using transmission electron microscopy. TEM and electron diffraction data from an Sb-catalyzed nanowire are shown in Figure 13. The inter-planar spacing of the nanowires grown using Sb was found to be 0.337 nm which corresponds to a lattice parameter of 0.583 nm. This matches well with published data on elemental Ge [23]. In addition, electron diffraction patterns were obtained from multiple locations along the length of a nanowire.

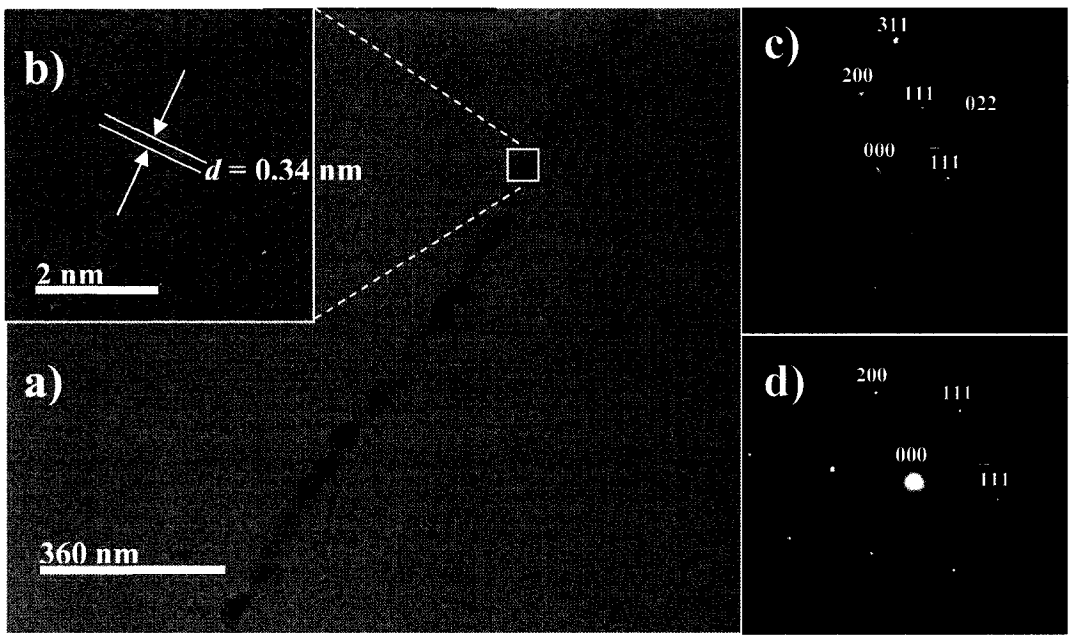

Figure 17. a) HRTEM image of an Sb-catalyzed Ge nanowire. b) Close packed planes of the Ge nanowire. c) and d) Electron diffraction patterns obtained from different locations along the length of the wire.

The diffraction patterns were indexed and confirmed to be from a diamond cubic crystal lattice as viewed along the <110> zone axis. Analysis of the diffraction patterns is included in Appendix C. From the diffraction patterns and the measured lattice constant, it can be said with reasonable certainty that the nanowires are elemental Ge and that they grew along the <111> direction. The diffractions patterns were identical at both the spheroid regions and the necking regions along the wire, indicating the unusual morphology of the nanowires did not alter their crystallography.

CHAPTER SIX

DISCUSSION

Semiconductor nanowires are being examined as possible replacements for current transistor channels and as platforms for studying physical phenomena in small objects, such as quantum confinement of electrons. This study focused on using materials currently used as dopants in the semiconductor industry as catalysts for growing Ge nanowires. This research is expected to help facilitate the adoption of Ge nanowires into current semiconductor manufacturing processes.

6.1 In-Catalyzed Ge Nanowires

The effects of growth temperature and catalyst thickness on the morphology and surface density of In-catalyzed Ge nanowires are discussed in this section. In addition, the crystallography and composition of the In-catalyzed Ge nanowires grown at 450 °C are compared to published data on elemental Ge and Ge nanowires and an attempt made to explain any discrepancies.

6.1.1 Temperature Effects

Before any discussion can be started about the results of this study, a formal definition of a nanowire must be given. In order to be classified as a nanowire in this study, a structure must have a diameter below 100 nm and above 10 nm with little to no variation, a length of at least 500 nm, and have no more than one kink per 200 nm of its length.

100 nm as the maximum allowable diameter was chosen because there will be little to no quantum confinement effects above this diameter. A diameter below 10 nm would make the nanowires too difficult to work with. Having a tapered diameter would cause the nanowire to have varying electrical characteristics along their length, which would render them unusable for device applications. The minimum length requirement and maximum number of kinks were selected because nanowires with these characteristics would be easy to deal with in future device studies.

In this study, In-catalyzed Ge nanowires were only grown at 450 °C. In most published literature, nanowires that were grown at different temperature exhibited different characteristics [10]. In this study, no structures that could be classified as nanowires were found on any specimens processed under 450 °C when In was used as the catalyst. Instead, nanostructures resembling nanowires were present. Most of these structures appeared to have grown in a one dimensional manner. However the direction of their long axis is not uniform, resulting in crooked and meandering structures, like those in Figures 8d and 8e. These observations contradict the theory that one dimensional growth is predicated on the eutectic temperature of the binary system. The eutectic temperature of the Ge-In binary system is 125 °C. No nanostructures were observed at any temperature below 400 °C. Therefore, it is logical to conclude that there is a specific temperature that is necessary to maintain the kinetics for straight one-dimensional growth in this experimental system. Indeed, that this temperature is 450 °C is supported by the fact that Ge nanowires were only successfully grown in the same

experimental chamber between 430 °C and 480 °C when using Au as a catalyst. The eutectic temperature for that system is 360 °C.

On In-coated substrates processed above 450 °C, nanowires were replaced by whiskers. These structures were sometimes larger that a micron in diameter and tens of microns in length, as shown in Figure 8c. The tapered structure of these whiskers indicated three dimensional growth was occurring. The prevalence of these structures across the substrate at higher temperatures can be attributed to increased surface mobility of the catalyst at elevated temperatures. This has also been observed with Au colloids as catalysts for Si nanowire growth [29]. The extremely thick catalyst films would agglomerate into much larger droplets than those found using either Au colloids or Au thin films. These larger droplets would then determine the overall diameter of the structures growing beneath them.

6.1.2 Surface Density

The higher average surface density of Ge nanowires found on SiO_2 compared to Si(111) was not able to be fully explained at this time. It was thought that there were two primary interactions that could contribute to the difference in surface density. First, the surface energy of the Si(111) substrate would be higher than that of the SiO_2 substrate due to it being a close packed plane. Because of this, it was reasonable to assume the wetting angle between SiO_2 and In would be larger than that between Si(111) and In. It is also reasonable to assume that the molten droplets that formed on SiO_2 and Si(111) were approximately the same size because diameters of nanowires found across the two

substrates were nearly identical. Because the surface energy of the Si(111) is higher than the surface energy of the SiO_2 substrate, there will be a lower attraction between the catalyst and the Si(111) substrate, resulting in a higher rate of evaporation. This theory was invalidated when the vapor pressure of the catalyst was calculated at 450 °C. Equation 1 was used to determine the vapor pressure for In.

$$\log p = AT^{-1} + B\log T + CT + D \qquad \text{Equation 1}$$

Here, p represents the vapor pressure in torr of the film, T is the temperature in Kelvin, and A, B, C, and D are constants with values -12,860, -0.7, 0, and 10.7, respectively [30]. At 450 °C, T will equal 723 K. Plugging in these values to Equation 1 and taking the inverse log yielded a vapor pressure of 8.35×10^{-10} torr, or 1.11×10^{-10} Pa. This constitutes a miniscule atomic flux, which would not make up for the discrepancy in surface density between the two substrates.

The second possible source of catalyst loss was to diffusion. It was thought that some of the In atoms could migrate into the substrate creating a heavily doped layer below the surface of the substrate. In atoms could migrate through interstitial sites or vacancies in the Si(111) substrate. Conversely, the dominant mechanism for In migration through SiO_2 would be ionic vacancies. These would require significantly more energy to form than thermal vacancies in Si(111). Therefore, more In atoms would diffuse into the Si(111) substrate than the SiO_2. The diffusivity of In in Si(111) at 450 °C was calculated using the Arrhenius rate equation and found to be 5.584×10^{-19} cm^2s^{-1}.

Calculations for diffusivity are contained in Appendix D. From this, the flux of atoms moving through the substrate, J, can be calculated from Fick's first law of diffusion, shown as Equation 2.

$$J = -D\frac{dC}{dx} \qquad \text{Equation 2}$$

Here, dC is the change in concentration between the surface and some depth below the surface, dx. The maximum solid solubility of In in Si, 7.4×10^{19} cm^{-3} was used for the value of dC. This is because it is assumed that that is the maximum surface saturation achievable and that there is no indium in the substrate prior to growth. At a depth of ten nanometers, the flux of In atoms was calculated to be 4.12×10^{9} $cm^{-2}s^{-1}$. At this rate, approximately 2.97×10^{13} atoms would be lost to diffusion into the substrate during the two hour growth period. Estimating that the specimen is 1 cm^2 with a catalyst film 30 nm thick, then there are approximately 9.5×10^{18} atoms in the film. Loss from diffusion into the substrate would account for far less than a fraction of a percent of the total amount of catalyst on the surface of the substrate.

With both theories proven not to be the cause of the catalyst loss, there is not sufficient evidence to draw a definitive conclusion as to why there is a significant difference in the surface density between the two substrates. The simplest possible reason for the difference in surface density lies in the deposition of the catalyst. Since no measurement was made of the thin film thickness prior to growth of Ge nanowires, it is possible that the measurement device in the sputtering chamber was not calibrated

properly. This is supported by the fact that the Si(111) specimens and the SiO_2 specimens were prepared at a different times. This could also be the cause of the lack of nanowires on substrates with thinner layers of catalyst.

6.1.3 Crystallography

The crystallography of the majority of the In-catalyzed nanowires agreed with published data on Ge nanowires grown in this temperature range. As previously stated, all of the wires grown on SiO_2 and ten of the twelve nanowires grown on Si(111) grew along the <111> direction. Measurements of the distance between consecutive lattice planes yielded a lattice constant of 0.571 nm. It is thought that the remaining two wires grew along the <112> direction, which was also seen in the research of Mathur *et al.*, though no substantial explanation for the kinetics of this growth direction were given [15]. The <112> direction had also been seen in Si nanowires grown using an oxide assisted method [29]. Tan *et al.* developed a theory to explain the kinetics of growth in this direction [19]. They theorized that growth in the <112> direction was predicated on the presence of a pair of Schockley, or partial, dislocations. These dislocations are at 30° to each other and produce a screw dislocation in the {111} plane. The screw dislocation causes the [111] planes to grow in a series of steps. These steps are what allow the wire to grow along the <112> direction. The wire then grows in a spiral around a screw dislocation [19].

The lattice planes of the <112> nanowires were measured and found to be 0.473 nm, which does not correspond to any lattice plane spacing for elemental Ge. However,

it does correspond with measurements taken from images published by Mathur *et al.*, which showed nanowires with lattice spacing of 0.465 nm [17]. No explanation was given for this discrepancy from published data on Ge and there is not enough evidence to postulate an explanation here.

6.1.4 Compositional Analysis

EDS measurements were taken at the interface of the wire and the catalyst tip. The measurements showed peaks corresponding to O, Ge, Si, Cu, and In. The O, Si, and Cu peaks were determined to be from the TEM grid by taking a measurement from a field with no nanowires. The measurements confirm that the nanowires grew using In as a catalyst. Successive EDS measurements from other nanowires without visible catalyst tips showed no presence of In. There is the possibility that traces of In diffused down the length of the nanowire. However, because the solid solubility of In in Ge is approximately 0.009 atomic percent, which is below the detection capabilities of EDS, this could not be confirmed. Confirmation for this could be obtained by measuring the electrical conductivity of the wires and comparing the results with published information on elemental Ge. An elevated conductivity using a positive bias would indicate that the wires were electrically doped by the In. There may be further discrepancies between the wires and published data on elemental Ge because of quantum confinement effects. These could be corrected by comparing the results to published research on Au-catalyzed Ge nanowires.

6.2 Sb-Catalyzed Ge Nanowires

The effects of growth temperature, substrate selection, and catalyst thickness on the morphology and surface density of Sb-catalyzed Ge nanowires are discussed in this section. In addition, a theory to explain the beaded morphology found in the Sb-catalyzed Ge nanowires grown in this study, with supporting evidence from published data on Si nanowires, is presented.

6.2.1 Temperature Effects, Crystallography, and Compositional Analysis

Sb-catalyzed nanowire growth occurred at temperatures higher than those for In-catalyzed nanowires. This was not unexpected because the melting temperature of Sb is 630 °C and the Ge-Sb eutectic temperature is 587 °C. The morphology of the Sb-catalyzed nanowires did not change significantly across different temperatures. However, the most significant temperature effect was the overall morphology of the wires.

A distorted, bead-like morphology was observed in all Sb-catalyzed Ge nanowires. This kind of morphology was also found in Si nanowires that had been annealed at elevated temperatures. Peng *et al.* theorized that the cylindrical shape of the nanowires, with a high surface area to volume ratio, was thermodynamically unstable [29]. This would make them more susceptible to surface tension effects. Annealing or growth of Si nanowires (at 1300 °C or higher) above the normal growth temperature (1200 °C) caused the nanowires to form chains of Si nanospheres, connected to one

another by a SiO_2 bridge. They proposed that as the Si atoms migrated into the spheres, the SiO_2 sheath surrounding the wire core diffused in the opposite direction to form the interlinking bridges, effectively lowering the surface/interface energy of the system. A sphere, after all, has a much lower surface area than a cylinder of equal volume. During this process, it was proposed that the SiO_2 sheath was in a semi-liquid state, which is consistent with the suppressed melting temperatures found in nanomaterials. Peng *et al.* observed that the nanospheres had uniform radii, were separated by a uniform distance from one another, and that both of these characteristics could be controlled by the temperature the samples were annealed at [31].

In the study presented here, the spheroids are irregularly shaped and appear randomly along the length of the wire. In addition, HRTEM and electron diffraction patterns taken at different locations along the length of an Sb-catalyzed wire showed it was single crystalline along its entire length, including the bridge between the spheres. The Sb-catalyzed Ge nanowires grew between 610 °C and 670 °C, which is higher than Au and In-catalyzed Ge nanowires (~400-500 °C) in this system, and resulted in the spheroid morphology. However, the temperatures used here probably could not provide enough energy for the atoms within the wire to completely migrate into independent spheres compared to the spheroidization of Si nanowires at higher temperatures.

6.2.2 Surface Density

The highest surface density of Sb-catalyzed nanowires, 2.76 μm^{-2}, was found on SiO_2 specimens coated with 4 nm of Sb and processed at 650 °C. No definitive trend

could be determined from the data on the effects of processing parameters on the surface density of nanowire growth. Substrates coated with 4 nm of Sb produced the highest surface densities at all temperatures except for 610 °C. These statistics can be deceiving, however, because of the high standard deviation found in the specimens processed at 610 °C. The standard deviation of the sample from every catalyst thickness processed at 610 °C was nearly equal to their average surface density. This would indicate a very low level of confidence in the data. Therefore, more data should be collected to provide a more precise analysis of the effects of processing specimens at 610 °C. The standard deviation of the samples coated with 4 nm of Sb and processed at 630 °C and 670 °C was also at least double that of the samples with thicker catalyst films processed at the same temperatures. From the data, the best conclusion that can be made is that the sample coated with 4 nm of Sb and processed at 650 °C showed the highest yield at $2.76 \pm 0.03\ \mu m^{-2}$ with a 95% confidence interval.

No nanowires were found on any of the Si(111) substrates or SiO_2 substrate coated with less than 4 nm of Sb. It was thought that the reason for the lack of growth on these substrates was caused by the catalyst was being lost before nucleation could occur. Like with the In-coated specimens, the loss of catalyst was again thought to be caused by either evaporation or diffusion into the substrate. The vapor pressure was evaluated for Sb using Equation 1 and found to be 3×10^{-3} torr, or 0.40 Pa. The atomic flux, Φ_0, can be calculated from the vapor pressure, p, using Equation 3 [30].

$$\Phi_0 = \frac{p}{\sqrt{2\pi m k_B T}} \qquad \text{Equation 3}$$

Here, m is the atomic mass, k_B is Boltzmann's Constant in $J \cdot K^{-1}$, and T is the temperature in Kelvin. Using the vapor pressure calculated above and 923 K for T, the flux is 3.143×10^{17} $cm^{-2}s^{-1}$. For a 1 cm^2 specimen processed for two hours, there will be 2.263×10^{21} atoms lost from evaporation. A film 10 nm thick on the same specimen would equal 1.095×10^{19} atoms. Therefore, the catalyst film could have evaporated before nucleation could occur. This calculation was based on kinetic motion of particles in spherical coordinates, which is why there is a factor of 2π in the denominator. Therefore, this calculation is slightly higher than what would be found from one dimensional evaporation of particles. However, this would not significantly change the huge flux as calculated above.

Substrate diffusion was also examined as a possible cause of catalyst loss. Diffusion into the substrate was again calculated using Fick's first law. The diffusivity of Sb into Si(111) at 650 °C was calculated to be 3.141×10^{-13} cm^2s^{-1}. Again, it was assumed there was no Sb present in the substrate prior to processing and the surface layer was at the maximum solid solubility achievable, 2.872×10^{21} cm^{-3}. The flux 10 nm below the surface was then calculated to be 9.020×10^{16} $cm^{-2}s^{-1}$. For a specimen 1 cm^2 and processed for two hours, this would mean 6.494×10^{20} atoms had diffused into the substrate. A film 10 nm thick on the same specimen would equal 1.095×10^{19} atoms. Therefore, it is conceivable that the Sb catalyst diffused into the substrate before nucleation could occur. Combining this result with the calculation of catalyst evaporation, it is highly probable the catalyst was lost before nucleation of Ge nanowires could occur on Si(111).

It should be noted that the thickness of neither the In nor Sb catalyst films were ever verified externally of the sputter chamber. The films thicknesses reported here were recorded from a crystal detector positioned in the chamber within the flux of the sputtered material. The detector measured the flux of material and used this to calculate a deposition rate. The detector was calibrated prior to deposition for each independent metal. However, these calibrations should have been verified using a surface measurement technique such as atomic force microscopy. Therefore, the catalyst thicknesses reported here may not be accurate. Instead, the thicknesses reported are nominal values and are accurate as far as their ratios relative to one another.

CHAPTER 7

CONCLUSIONS

The motivation behind this research was to determine if metals commonly used in the semiconductor industry as dopants can be used to catalyze semiconductor nanowire growth. This would significantly improve the likelihood of integrating semiconductor nanowires into future semiconductor devices because current catalyst materials like gold are viewed as a contaminant in existing manufacturing processes. In addition, the use of a dopant material as a catalyst makes it a likely source for doping the wires after growth, eliminating the need for incorporating additional gases during the growth process which may complicate the nucleation process.

For this experiment, In and Sb were evaluated as potential catalysts for Ge nanowire growth. Si(111) and SiO_2 substrates coated with 25 nm and 30 nm of In yielded Ge nanowire growth when processed at 450 °C. In-catalyzed Ge nanowires grew with a higher surface density on SiO_2 than Si(111). SiO_2 substrates coated with Sb films greater than or equal to 4 nm also yielded Ge nanowire growth when processed between 610 °C and 670 °C. The highest surface density of Sb-catalyzed Ge nanowires was found on an SiO_2 substrate coated with 4 nm of Sb and processed at 650 °C. Both In-catalyzed and Sb-catalyzed Ge nanowires grew predominantly along the <111> direction. All of the nanowires were confirmed to be elemental Ge through EDS measurements, or electron diffraction and calculations of the lattice constant.

From the data, it can be concluded that In and Sb can be used effectively to catalyze Ge nanowire growth. In addition, it was shown that SiO_2 is a more suitable

substrate for Ge nanowire growth than Si(111), which would make future device integration easier. From the TEM data, it can be said that the <111> direction is the preferential growth direction for Ge nanowires grown using In and Sb as catalysts with the VLS process.

CHAPTER 8

RECOMMENDATIONS FOR FURTHER RESEARCH

Because the purpose of this research was to improve the possibility of incorporating semiconductor nanowires into electronics, the most glaring deficiency with this research is the lack of electrical measurements of the wires themselves. Electrical measurements should be conducted on as grown wires and wires that were annealed after growth for different periods of time. There should be a control group to compare against as well, which could be Ge nanowires grown with Au as a catalyst. This way the electrical measurements of the wires could determine whether or not catalyst diffusion doping can occur and if it occurs during growth or requires a post growth anneal.

Along with electrical measurements of the wires, In and Sb should be deposited at patterned sites on the same substrate. By using a deposition process like that used by Wand and Dai, In and Sb-catalyzed Ge nanowires could possibly be grown simultaneously on the same substrate. This would allow for the design of Ge nanowire based complementary metal oxide semiconductor (CMOS) devices. CMOS devices are the primary architecture of all logic and memory devices used today.

In addition to including the electrical characterization of In and Sb-catalyzed nanowires and patterned catalyst deposition, research should be conducted on the synthesis of In and Sb nanoparticles. These could then be used as catalyst sites without the need to coat the substrates with a thin film. In studies conducted with Au nanoparticles, the diameter of Ge nanowires was much more controllable. In addition, it has been shown that nanoparticles melt at significantly lower temperatures than bulk

materials. This could allow Sb-catalyzed Ge nanowires to be grown at lower temperatures, possibly eliminating the pearl like morphology observed in this study. It could also provide a controllable platform for studying the size effects on quantum confinement within the nanowires.

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APPENDIX A

INTERPLANAR SPACING CALCULATIONS

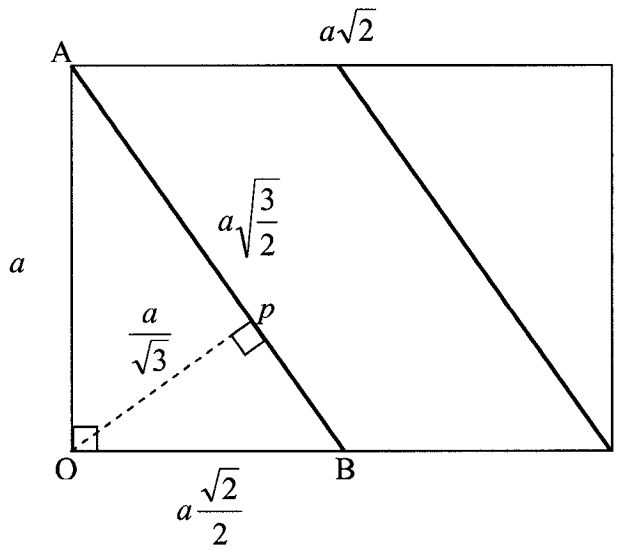


Figure 18. Diagram of the intersection of multiple parallel {111} planes with a {110} plane of a FCC crystal structure. {111} planes are colored blue.

The interplanar spacing of the {111} planes can be calculated with basic geometry. First, the length of Line Segment AB must be calculated using the Pythagorean Theorem:

$$a^2 + \left(\frac{a\sqrt{2}}{2}\right)^2 = \left\|\overline{AB}\right\|^2$$

$$\left\|\overline{AB}\right\| = a\sqrt{\frac{3}{2}}$$

Next, a line segment is drawn from the origin to a Point *p* on making a 90° angle with Line Segment AB. This creates a new triangle, OB*p*, which is similar to triangle OAB.

The ratio of the two triangles can be calculated by dividing line segment OB by line segment AB:

$$\frac{a\frac{\sqrt{2}}{2}}{a\sqrt{\frac{3}{2}}} = \frac{1}{\sqrt{3}}$$

The value of O*p* is calculated by multiplying the length of line segment OA by this value, resulting in $\frac{a}{\sqrt{3}}$. For Ge with a lattice constant of a = 5.658 Å, this gives a distance of 3.27Å between parallel {111} planes.

APPENDIX B

INTERPLANAR ANGLE CALCULATIONS

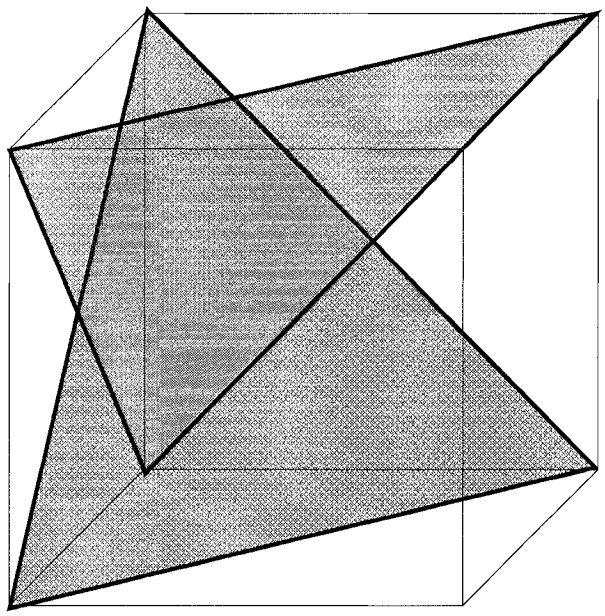


Figure 19. Alternating (111) planes in a cubic lattice.

For this derivation, the blue plane seen above is the (111) plane, while the red plane is the $(1\bar{1}\bar{1})$ plane.

To determine the angle between any two planes, the normal vector to each plane must be calculated. The normal vector of a plane is found by taking the cross product of two vectors within the plane.

For the (111) plane, the normal vector is:

$$[\bar{1}10]\times[\bar{1}01]=\begin{bmatrix} i & j & k \\ -1 & 1 & 0 \\ -1 & 0 & 1 \end{bmatrix}=(1-0)i-(-1-0)j+(0+1)k=i+j+k$$

For the $(11\bar{1})$ plane, the normal vector is:

$$[110]\times[101]=\begin{bmatrix} i & j & k \\ 1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}=(1-0)i-(1-0)j+(0-1)k=i-j-k$$

The angle between two lines can be found by taking of their dot product:

$$(i+j+k)\bullet(i-j-k)=\|i+j+k\|\cdot\|i-j-k\|\cos\theta$$

$$\theta=\cos^{-1}\left(\frac{1-1-1}{\sqrt{(1)^2+(1)^2+(1)^2}\cdot\sqrt{(1)^2+(-1)^2+(-1)^2}}\right)$$

$$\theta=\cos^{-1}\left(\frac{-1}{3}\right)=109.47°$$

APPENDIX C

INDEXING DIFFRACTION PATTERNS

When the orientation of the beam with respect to the zone axis is not known, a numerical method must be applied to determine the correct orientation. This requires the production of a pair of charts. The first chart consists of the ratios of the different interplanar spacings. This is achieved as follows:

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}}$$

The ratio of the interplanar spacings is then:

$$\frac{d_1}{d_2} = \frac{\sqrt{h_1^2 + k_1^2 + l_1^2}}{\sqrt{h_2^2 + k_2^2 + l_2^2}}$$

Table 8. A completed chart for the ratio of interplanar spacings in a diamond cubic crystal lattice.

	1/d(hkl)	(111)	(220)	(311)	(400)	(331)
1/d(hkl)		0.306232	0.500076	0.586391	0.353607	0.770668
(111)	0.306232	1	1.632993	1.914854	round	2.516611
(220)	0.500076		1	1.172604	0.707107	1.541104
(311)	0.586391			1	0.603023	1.314257
(400)	0.707214				0.5	1.089725
(331)	0.770668					1

The angles between the planes must also be known to complete the indexing:

$$\cos\theta = \frac{h_1 h_2 + k_1 k_2 + l_1 l_2}{\sqrt{h_1^2 + k_1^2 + l_1^2} \cdot \sqrt{h_2^2 + k_2^2 + l_2^2}}$$

Table 9. A completed table for the angles between several planes in the diamond cubic lattice.

	(111)	(220)	(311)	(400)	(331)
(111)	0	35.26439	29.49621	54.73561	22.00171
(220)		0	31.48215	45	13.26268
(311)			0	25.2394	25.94312
(400)				0	46.50848
(331)					0

Once two diffraction spots have been properly indexed, the rest of the spots can be determined through vector addition, shown in Figure 14:

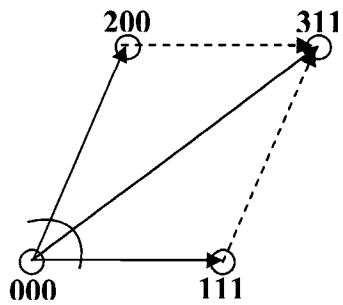


Figure 20. Indexing a diffraction pattern using vector addition

APPENDIX D

SOLID STATE DIFFUSIVITY CALCULATIONS

Solid state diffusivity calculations were based on the following equation:

$$D = D_0 \exp\left(\frac{-E_A}{k_B T}\right) \qquad \text{Equation 3}$$

D_0 is the diffusion constant for the solute in the solvent, E_A is the activation energy for atomic migration in eV, k_B is Boltzmann's Constant = 8.617×10^{-5} eV•K^{-1}, and T is the temperature the diffusion is taking place at in Kelvin.

For In diffusing into Si(111) between 600 °C and 850 °C:

$D_0 = 3 \times 10^{-2}$ cm^{2}s^{-1}

$E_A = 2.4$ eV

$D_{450} = 5.584 \times 10^{-19}$ cm^{2}s^{-1}

For Sb diffusing into Si(111) between 600 °C and 850 °C:

$D_0 = 4.0$ cm^{2}s^{-1}

$E_A = 2.4$ eV

$D_{650} = 3.141 \times 10^{-13}$ cm^{2}s^{-1}

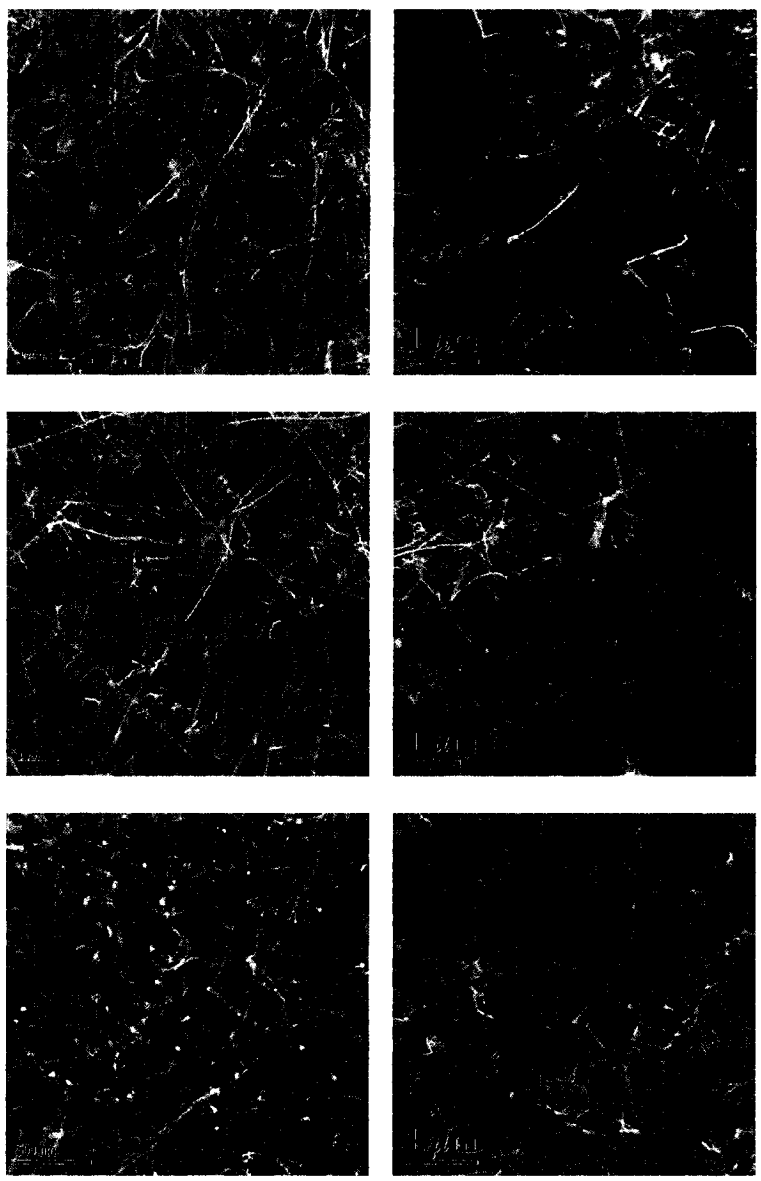
Values were obtained from the CRC Materials Science and Engineering Handbook [33].

APPENDIX E

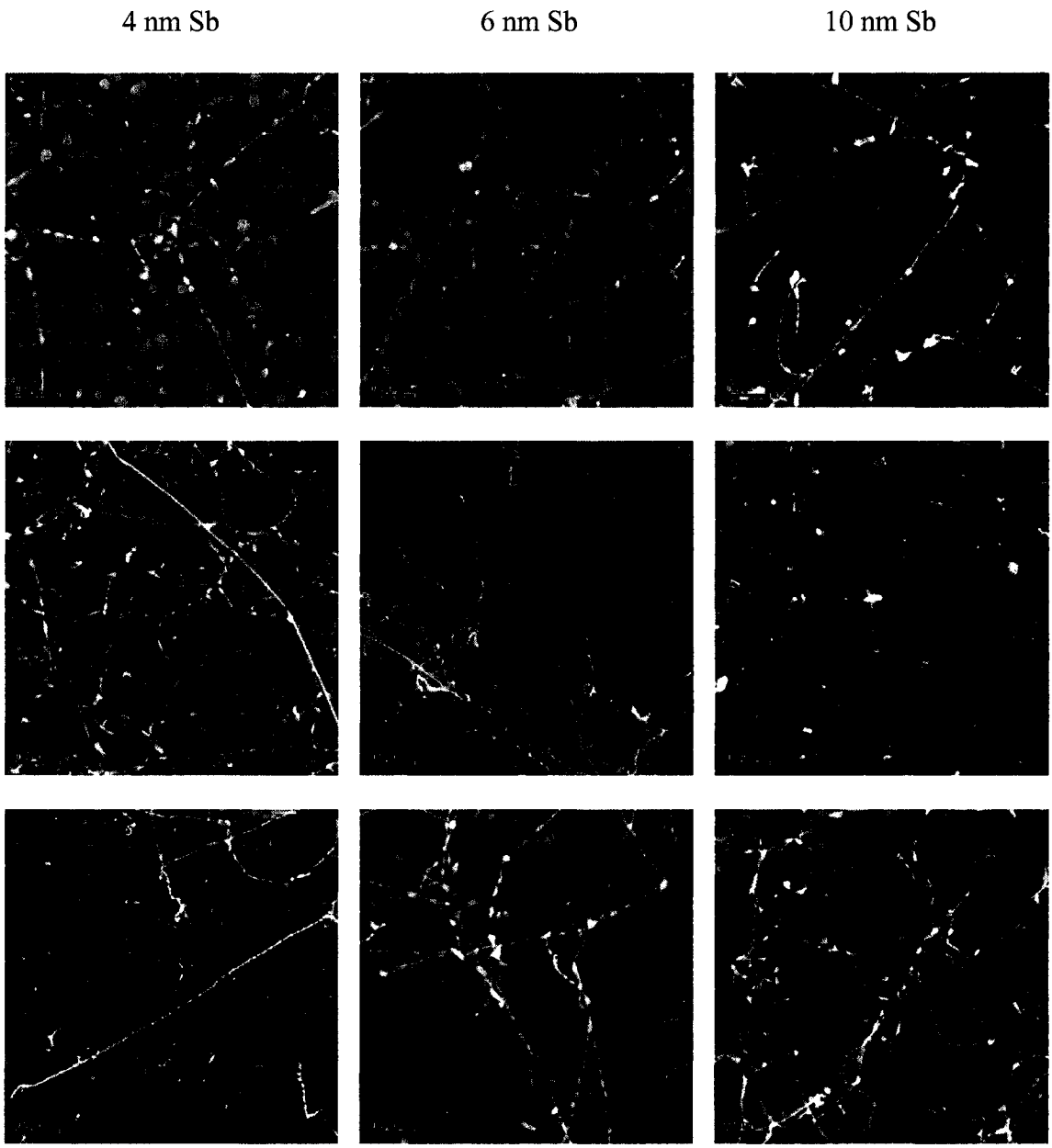
NANOWIRE SEM DATA FOR SURFACE DENSITY CALCULATIONS

In-catalyzed Ge nanowires grown at 450 °C.

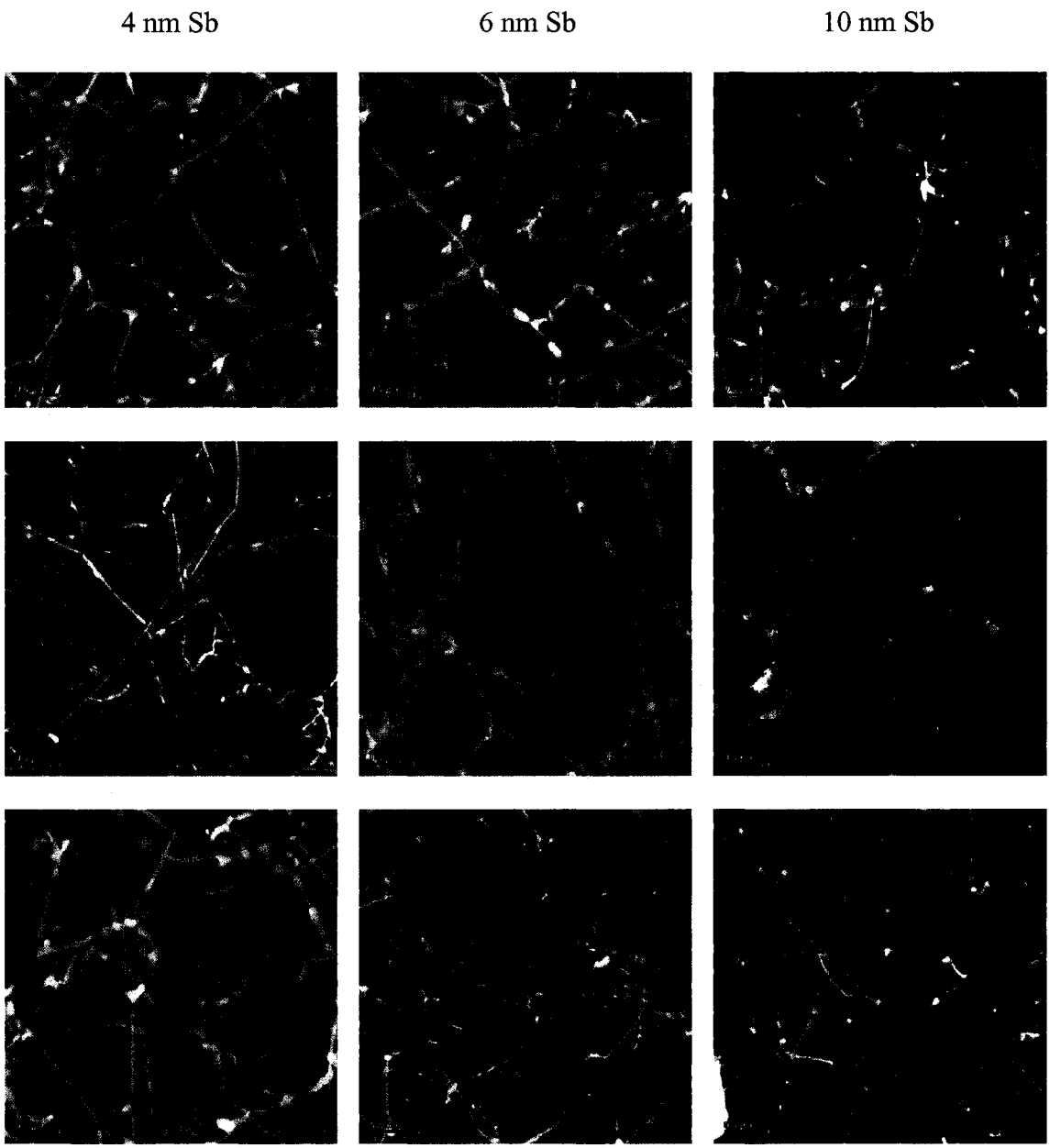
Substrate: SiO_2 Substrate: Si(111)



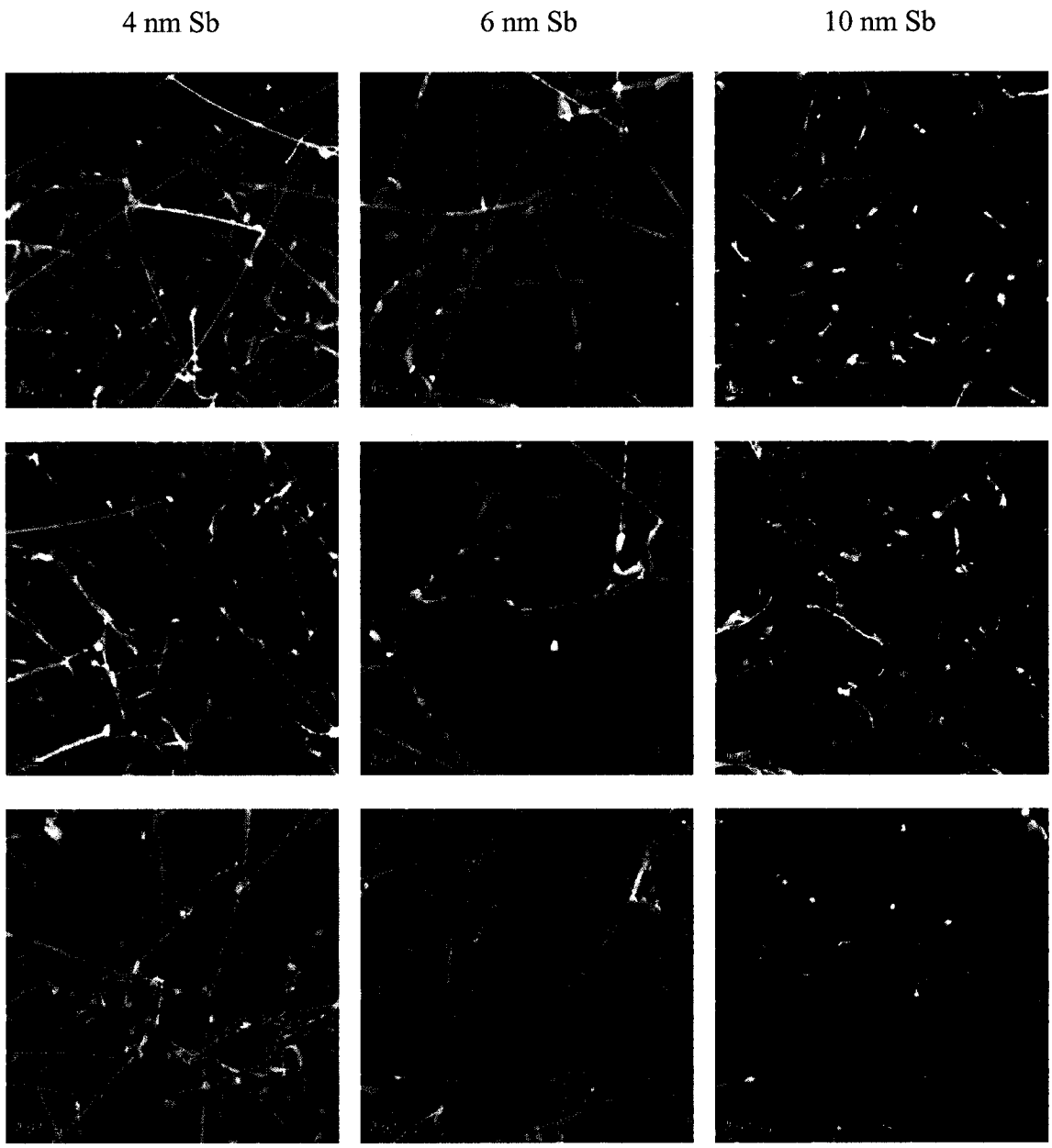
Sb-catalyzed Ge nanowires grown at 610 °C on SiO_2 substrates.



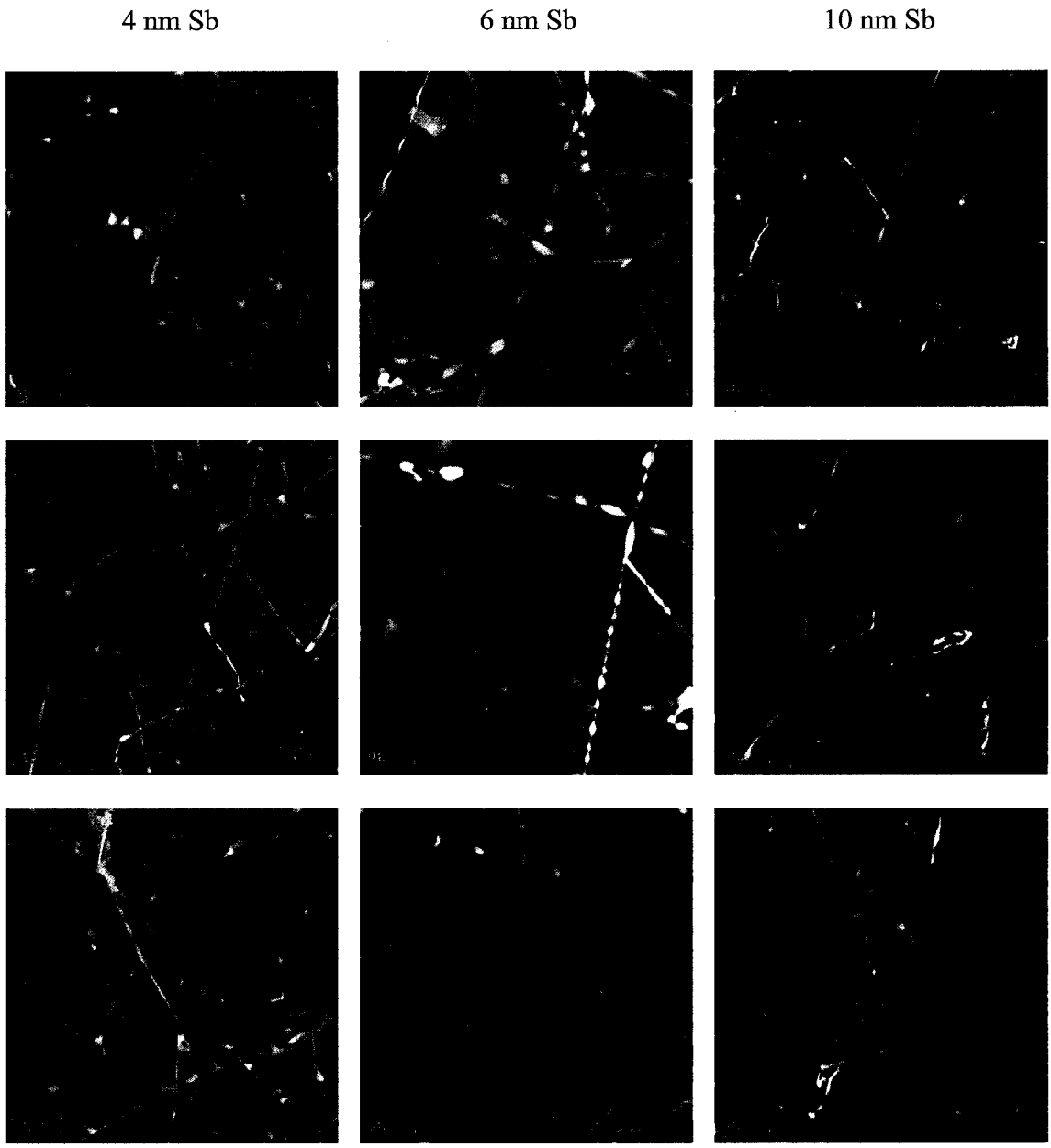
Sb-catalyzed Ge nanowires grown at 630 °C on SiO_2 substrates.



Sb-catalyzed Ge nanowires grown at 650 °C on SiO_2 substrates.



Sb-catalyzed Ge nanowires grown at 670 °C on SiO_2 substrates.



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